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Source: next-gen-forum.com

NEXT GENERATION SiC/GaN 3-Φ Variable Speed Drive Systems

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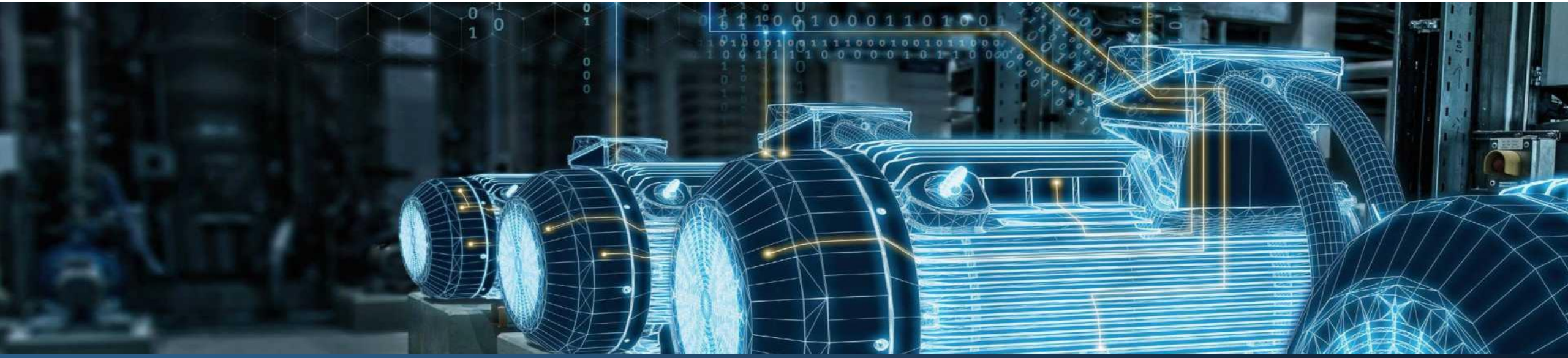
Source: SIEMENS



Next Generation SiC/GaN 3-Φ Variable Speed Drive Systems

Abstract — Variable-speed drive systems should feature high power density and low installation costs, offer wide input and output voltage/motor speed ranges, and ensure low EMI without requiring shielded motor cables. Accordingly, next-generation PWM inverters utilizing fast switching SiC/GaN power semiconductors should integrate LC output filters and/or generate continuous output voltages to prevent conducted or radiated EMI, reflections on long motor cables, high-frequency motor losses, dv/dt-related motor insulation stresses and bearing currents, such that conventional low-cost motor technology can be utilized.

The tutorial first analyses different dv/dt- and full-sinewave output filter concepts and highlights the advantages of multi-level voltage DC-link converter topologies regarding filter volume minimization. Next, the integration of inverter and motor is discussed, and a new phase-modular inverter concept (Y-inverter), extending the inverter functionality from buck to buck-boost operation, is introduced and subsequently condensed into a three-phase current DC-link inverter that employs a single-bridge-leg voltage-to-current DC/DC conversion input stage and advantageously utilizes novel four-quadrant switches in the DC/AC output stage. Next, starting from the basic DC/AC current DC-link topology a three-phase DC-link AC/AC converter concept is derived and also translated into a voltage DC-link concept following duality considerations. In a final step, indirect and direct AC/AC matrix converters without intermediate energy storage elements are introduced, followed by a discussion of multi-step commutation and space vector modulation schemes. A brief comparative evaluation of voltage/current DC-link and matrix AC/AC converter approaches concludes the tutorial.

Outline

- *Introduction*
- *SiC/GaN Application Challenges*
- *VSI with dv/dt-Filters*
- *VSI with Full-Sinewave Filters*
- *Multi-Level / Q2L /Modular VSI*
- *Buck+Boost VSI & CSI*
- *Indirect & Direct Matrix Converter*
- *Conclusions*

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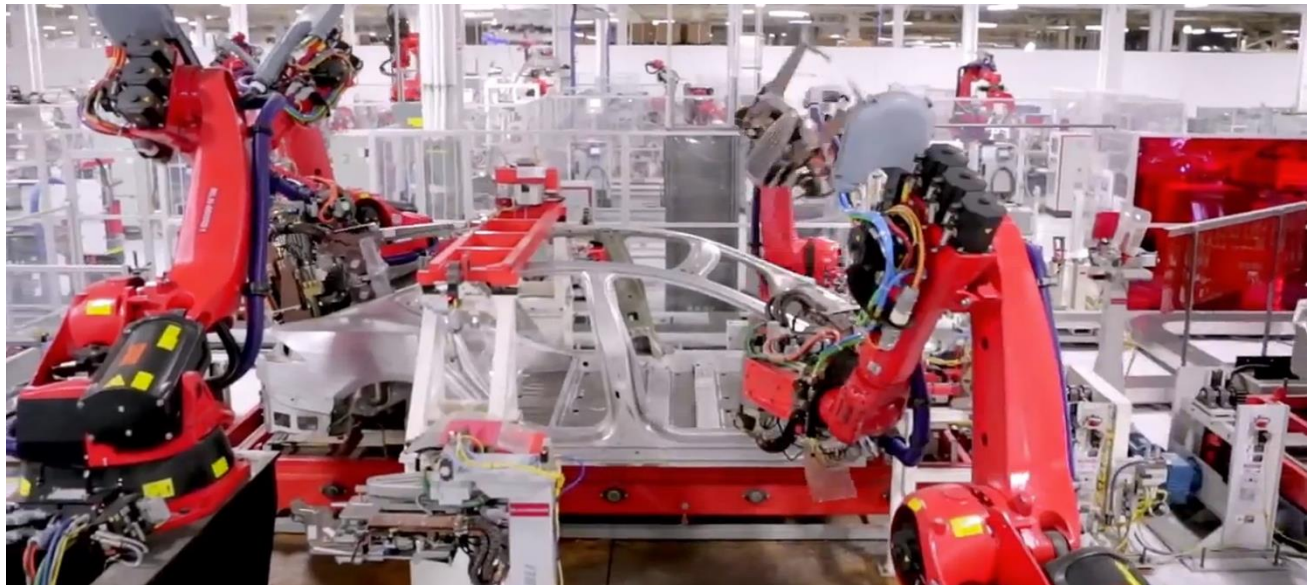
Variable Speed Motor Drive (VSD) Systems

- *Industry Automation / Robotics*
- *Material Machining / Processing – Drilling, Milling, etc.*
- *Compressors / Pumps / Fans*
- *Transportation*
- *etc., etc.* *.... Everywhere !*

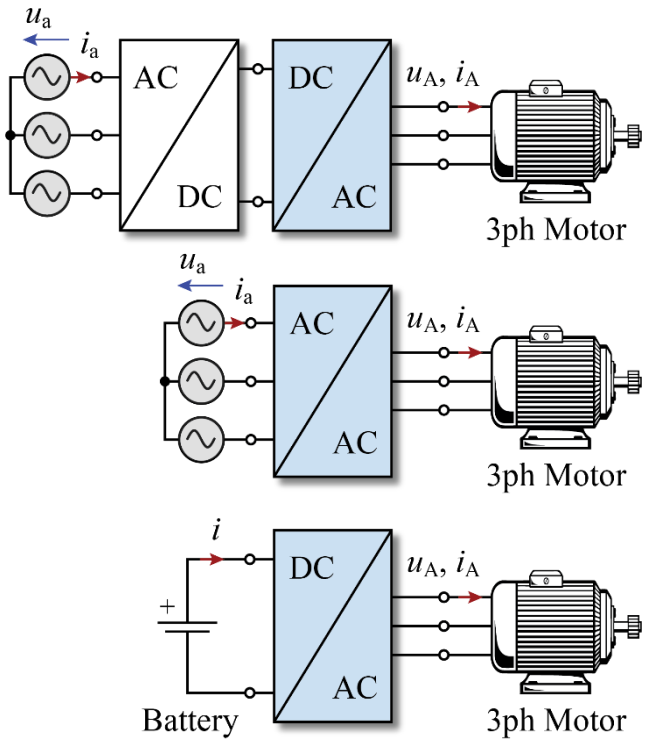


Source: TESLA MOTORS

- *60...70 % of All Electric Energy Used in Industry Converted by VSDs*

Variable Speed Drives — State-of-the-Art 1/2

- *DC-Link Based AC/DC/AC OR Matrix-Type AC/AC Converters*
- *Battery OR Fuel-Cell Supply OR Common DC-Bus Concepts*



38%
of electric energy use is for motors in commercial buildings.

70%
of electricity consumed by industry is used in electric motor systems.

Source: ABB

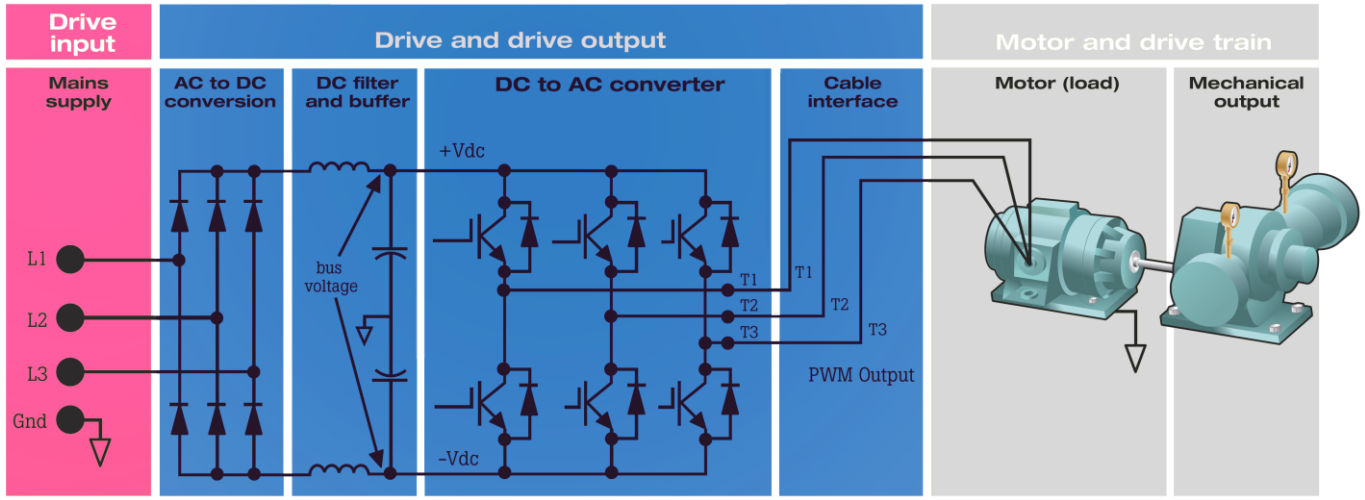
- *45% of World's Electricity Used for Motors in Buildings & Industrial Applications*

Variable Speed Drives — State-of-the-Art 2/2

- *Mains Interface | 3-Φ PWM Inverter | Cable | Motor → All Separated*
- *PWM Output → Conducted & Radiated EMI / Reflections @ Motor Terminals / Bearing Currents*

— *Large Installation Space / $$$*
— *Shielded Motor Cables / Filters / $$$*
— *Complicated / Expert Installation / $$$*

Source: FLUKE



- *High Performance @ High Level of Complexity & High Costs (!)*

SiC Low $R_{DS(on)}$ High-Voltage Devices

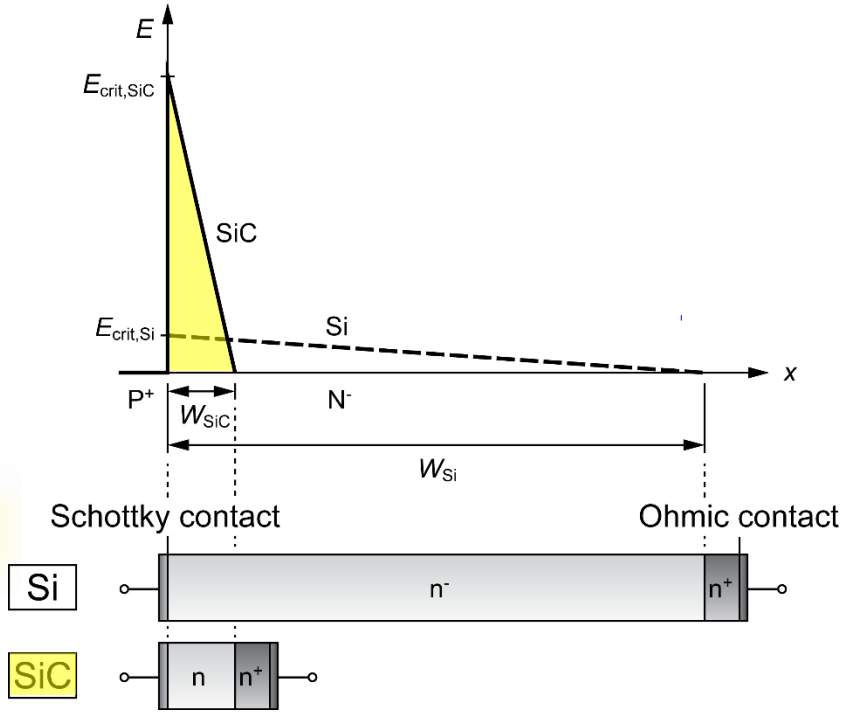
- *Higher Critical E-Field of SiC → Thinner Drift Layer*
- *Higher Maximum Junction Temperature $T_{j,max}$*

at 300 K	Si	GaAs	4H/6H-SiC	GaN
Eg (eV)	1.12	1.4	3.0-3.2	3.4
Ec (MV/cm)	0.25	0.3	2.2-2.5	3
μ_n (cm^2/Vs)	1350	8500	100-1000	1000
ε_r	11.9	13	10	9.5
vsat (cm/s)	$1x10^7$	$1x10^7$	$2x10^7$	$3x10^7$
λ (W/cmK)	1.5	0.5	3 - 5	1.3

$$R_{on}^{*} = \frac{4V_B^2}{\varepsilon\mu_n E_C^3} \leftarrow$$

For 1kV:	Si	SiC
W (μm)	100	10
N_D (cm^{-3})	10^{14}	10^{16}

$$R_{on,SiC}^{*} \approx \frac{1}{300} R_{on,Si}^{*}$$

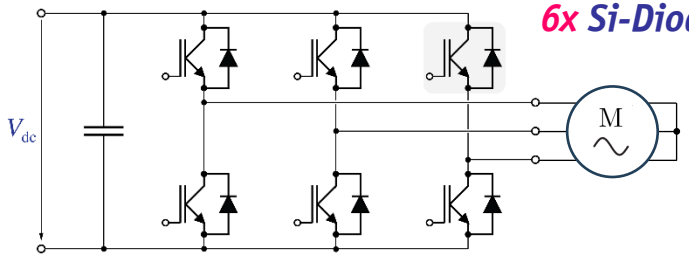


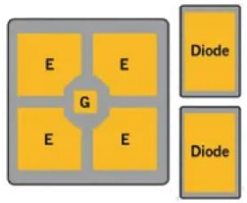
- *Massive Reduction of Relative On-Resistance → High Blocking Voltage Unipolar (!) Devices*

Si vs. SiC

- *Si-IGBTs / Diodes → Const. On-State Voltage, Turn-Off Tail Current & Diode Reverse Recovery Current*
- *SiC-MOSFETs → Loss Reduction @ Part Load BUT Higher R_{th}*

6x Si-IGBT
6x Si-Diode



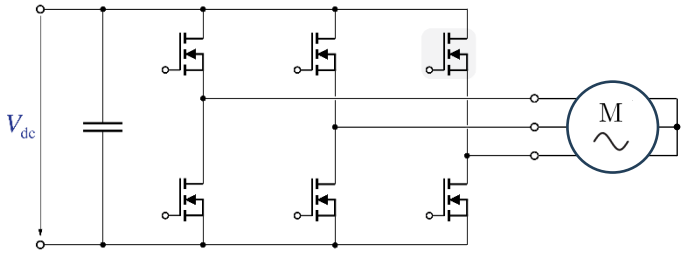


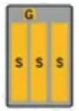
Source: ATZ elektronik

1200V 100A
Die Size: 98.8 mm² + 39.4 mm²

Source: Infineon

6x SiC-MOSFET





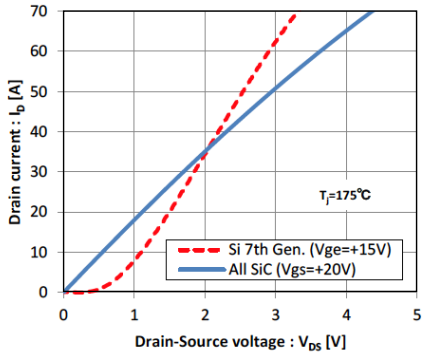
1200V 100A
Die Size: 25.6 mm²

Source: Cree

- *Space Saving of >30% on Module Level (!)*

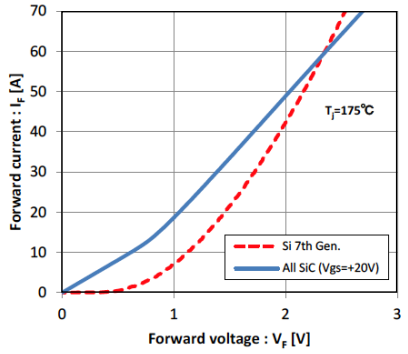
Si vs. SiC Conduction Behavior

- *Si-IGBTs / Diodes → Const. On-State Voltage Drop / Rel. Low Switching Speed*
- *SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed*

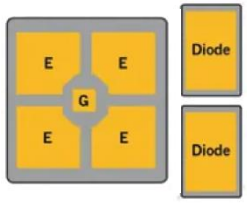


Source: Fuji Electric

Forward

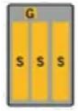


Reverse



1200V 100A
Die Size: 98.8mm² + 39.4mm²

Source: Infineon



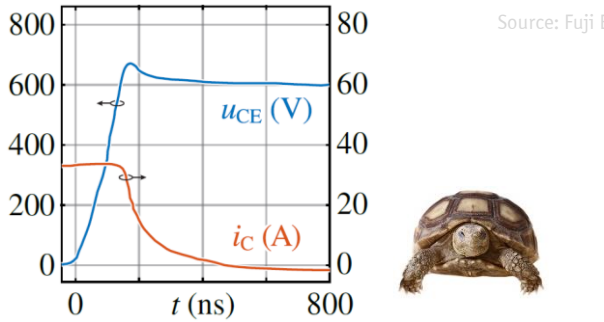
1200V 100A
Die Size: 25.6mm²

Source: Cree

- *SiC MOSFETS Facilitate Higher Part Load Efficiency*

Si vs. SiC Switching Behavior

- *Si-IGBTs / Diodes → Const. On-State Voltage Drop / Rel. Low Switching Speed*
- *SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed*



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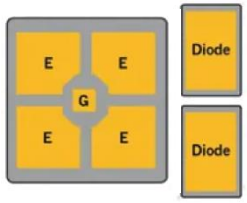
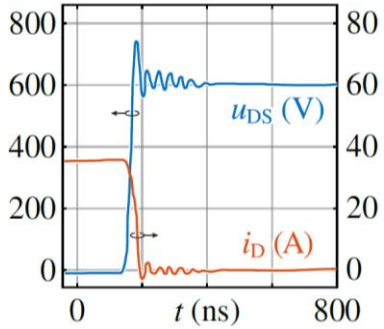
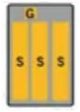


1200V 100A
Die Size: 98.8mm² + 39.4mm²

Source: Infineon



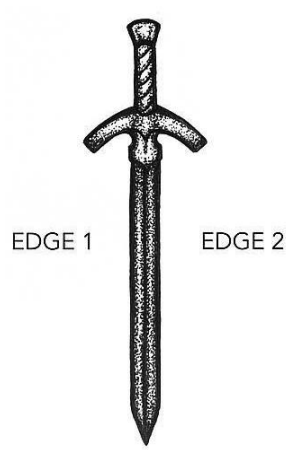


1200V 100A
Die Size: 25.6mm²

Source: Cree

- *High di/dt & dv/dt → Challenges in Packaging / EMI / Motor Insulation / Bearing Currents*

Challenges

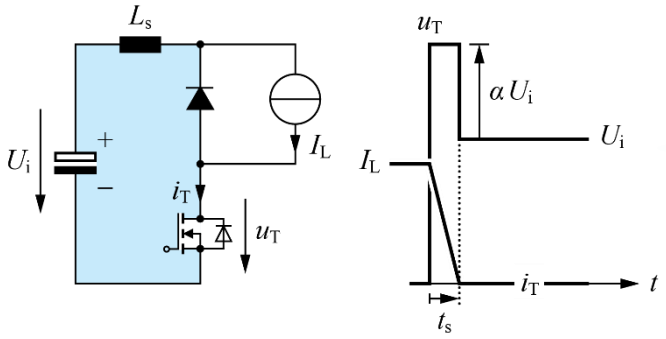


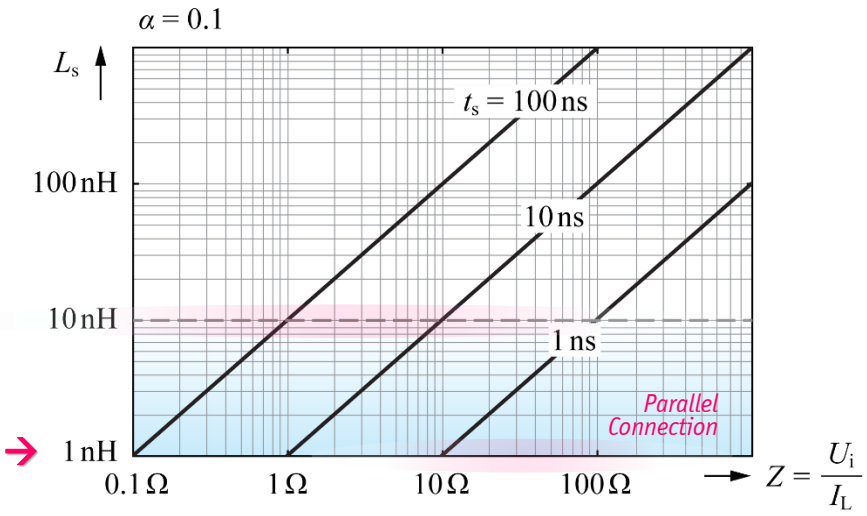
Low Commutation Loop Inductance

$$L\frac{di}{dt} = u$$

- *High di/dt Switching Transition*
- *Commutation Loop Inductance L_s*
- *Allowed L_s Directly Related to Switching Time t_s* →

$$L_s \le \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \frac{U_i}{I_L} \qquad z$$

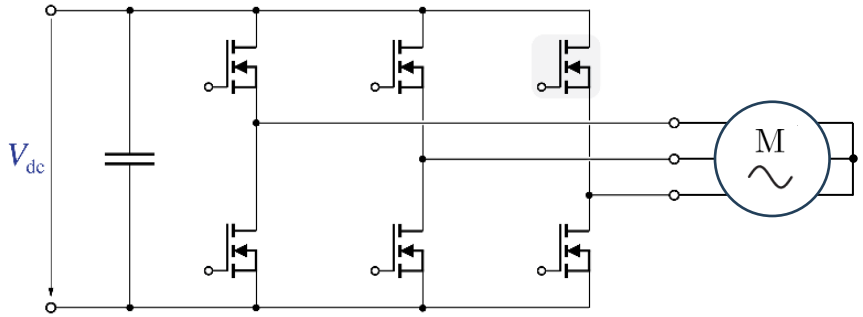




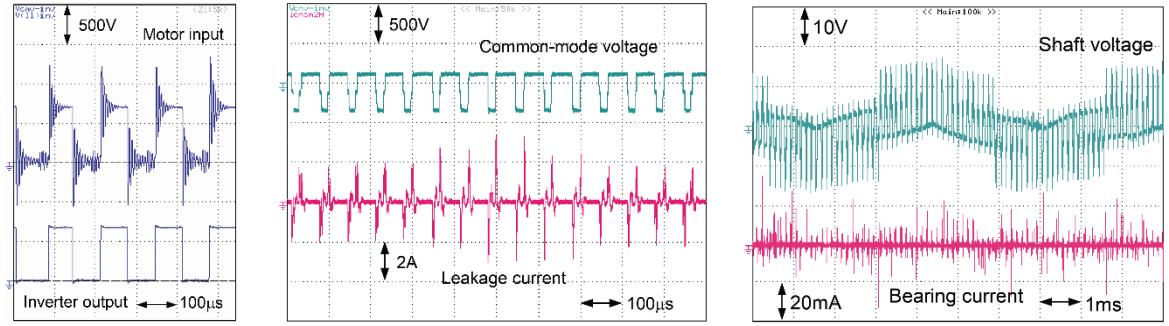
- *Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents (Z-Matching)*

Surge Voltage Reflections & CM Currents

- *High dv/dt / Short Rise Times of Inverter DM & CM Output Voltage Pulses*
- *Reflections @ Motor Terminals → High Insulation Stress*
- *CM Leakage Current → Radiated Emissions & Bearing Currents*



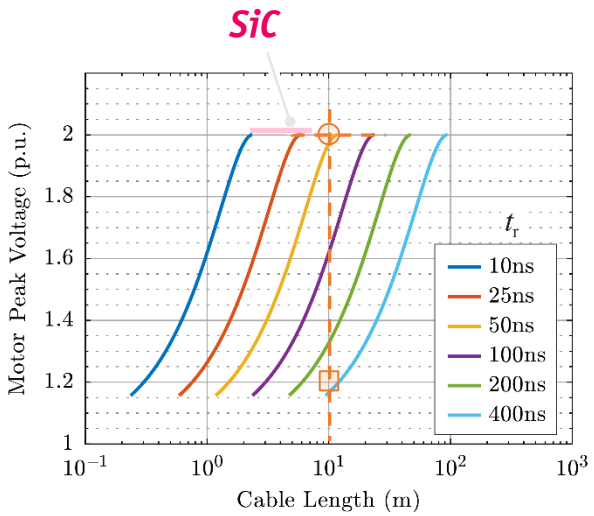
Source: YASKAWA



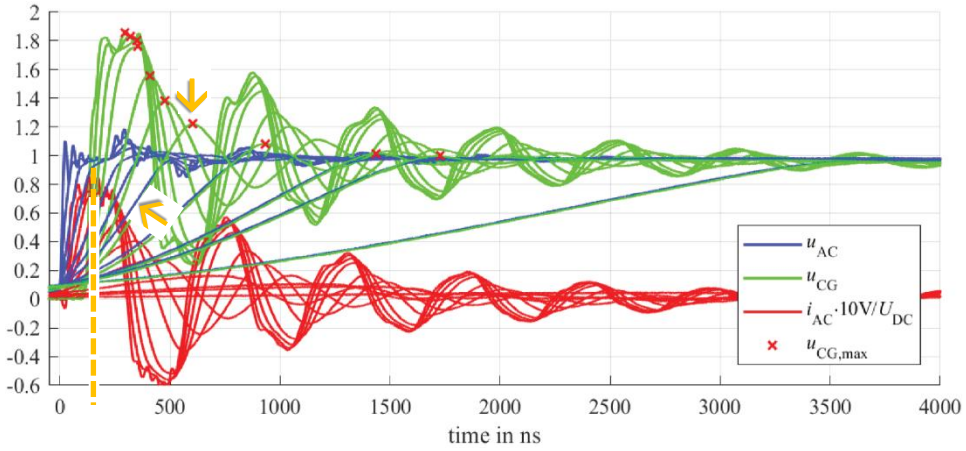
- *Motor Surge Voltage | CM Leakage Current | Bearing Current*

Surge Voltage Reflections

- *"Long Motor" Cable $l_c \geq \frac{1}{2}\, t_r\, v$*
- *Short Rise Time of Inverter Output Voltage*
- *Impedance Mismatch of Cable & Motor → Reflect. @ Motor Terminals / High Insul. Stress*



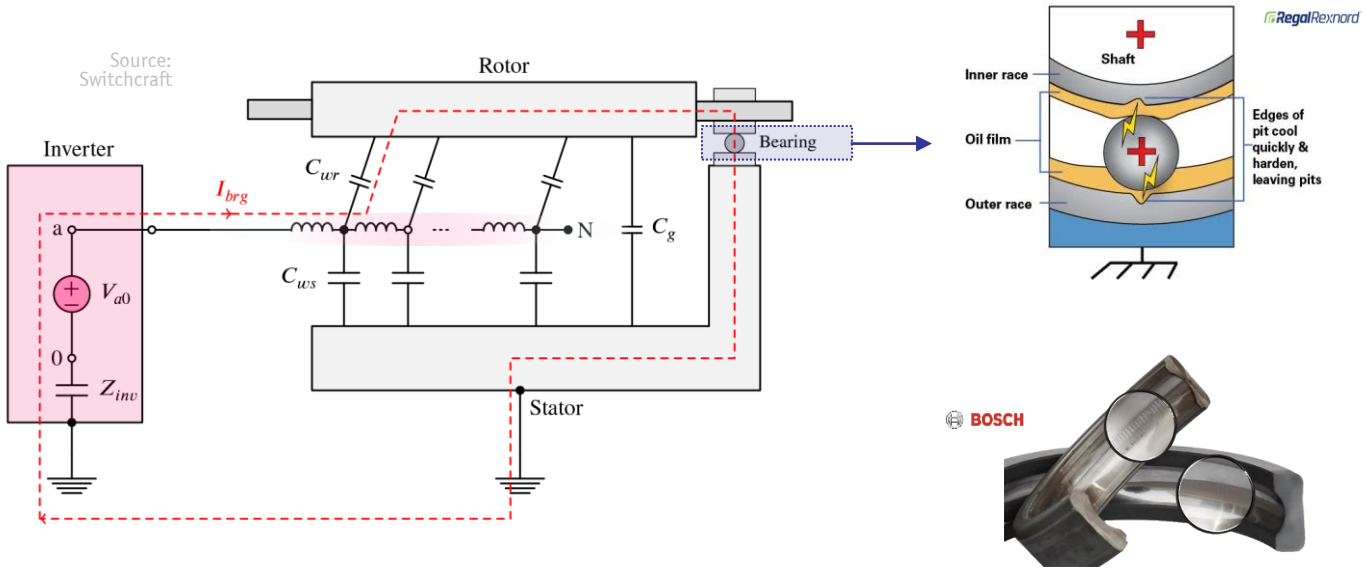
Source: Bakran / ECPE 2019



- *dv/dt-Filtering OR Full-Sinewave Filtering / Termination & Matching Networks etc.*

Motor Bearing Currents

- *Switching Frequency CM Inverter Output Voltage → Motor Shaft Voltage*
- *Electrical Discharge Machining ("EDM") in the Bearing*



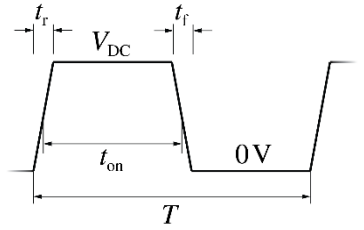
- *Cond. Grease / Ceram. Bearings / Shaft Grndg Brushes / dv/dt-Filter OR Full-Sinewave Filters*

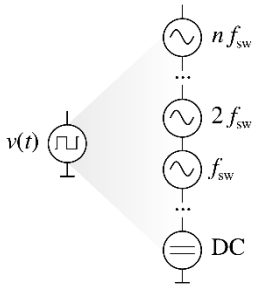
Conducted & Radiated EMI Emissions

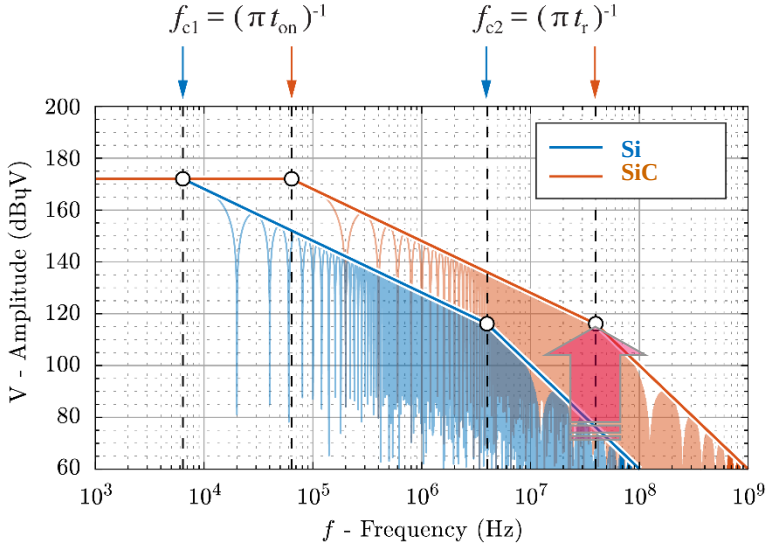
- *Higher dv/dt → Factor 10*
- *Higher Switching Frequencies → Factor 10*
- *EMI Envelope Shifted to Higher Frequencies*

f_S= 10 kHz & 5 kV/us for (Si IGBT)
f_S= 100 kHz & 50 kV/us for (SiC MOSFET)

V_{DC} = 800V
DC/DC @ D= 50%







- *Higher Influence of Filter Component Parasitics & Couplings → Advanced Design*

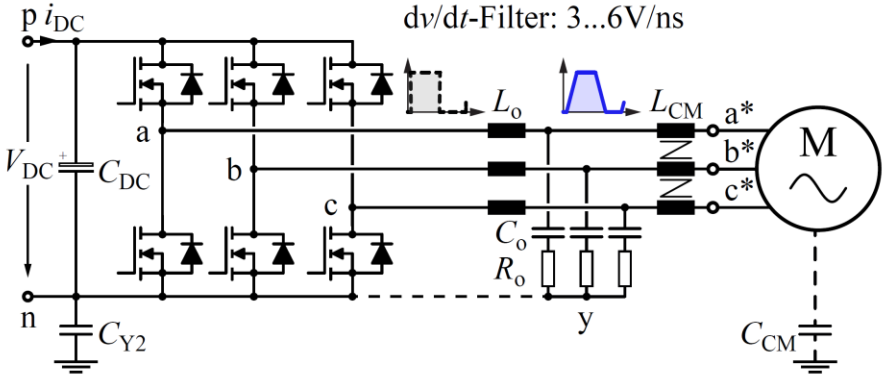
Inverter Output Filters

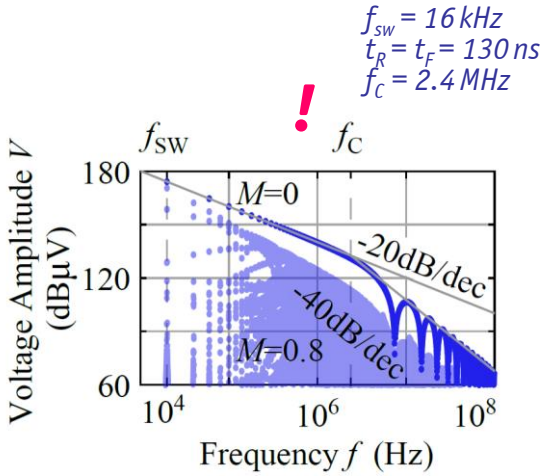
dv/dt-Filters
Full-Sinewave Filters

dv/dt-Limitation

Passive | Hybrid | Active dv/dt-Limitation

- *Passive – Damped LC-Filter $f_C > f_S$*
- *Hybrid – Undamped LC-Filter & Multi-Step Sw. Transition*
- *Active – Gate-Drive Based Shaping of Sw. Transients*

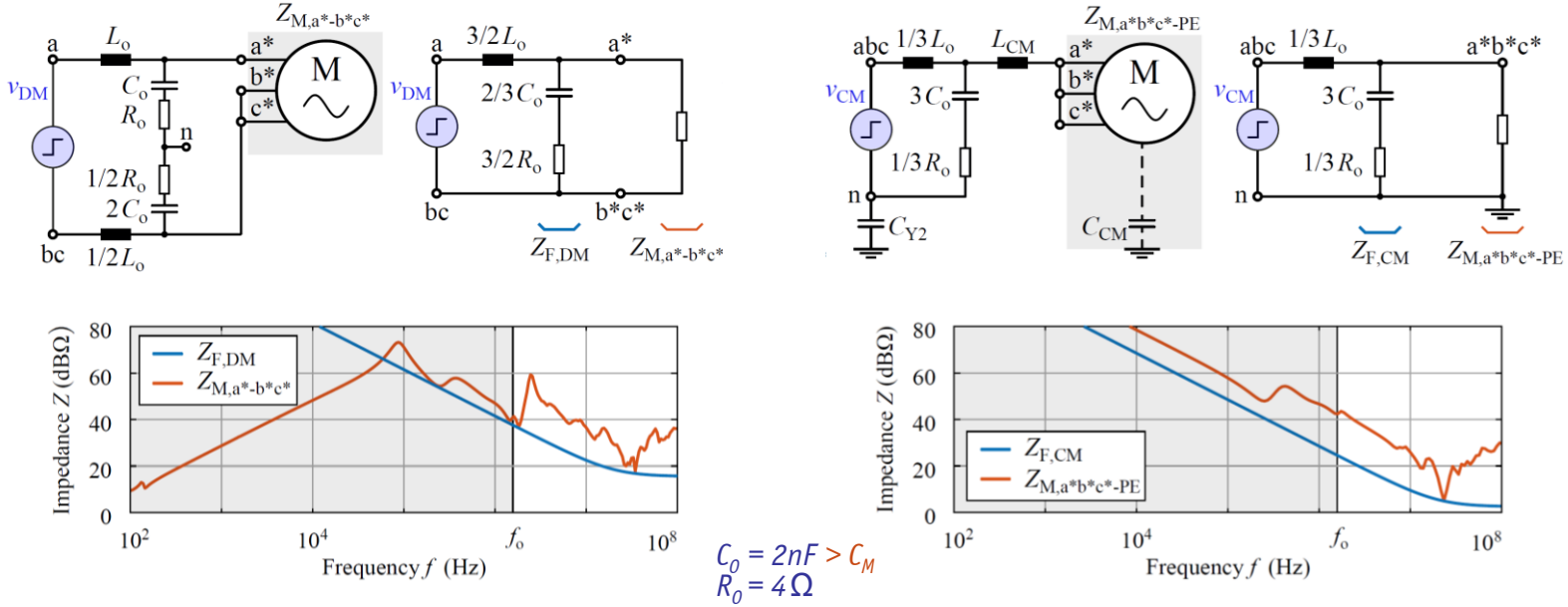




- *Connection to DC-Minus & CM Inductor → Limit CM Curr. Spikes / EMI / Bearing Currents*

Design of Passive dv/dt-Filters

- *Influence of Motor Impedance Z_M & (Long) Motor Cable*
- *Sw. Transient — Results in DM & CM Voltage Step → Consider DM & CM Properties*

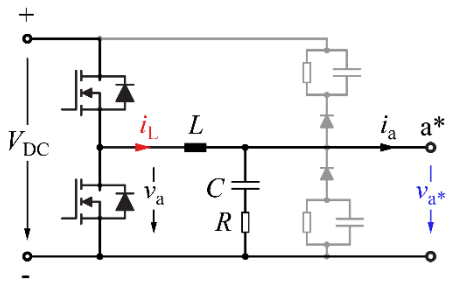


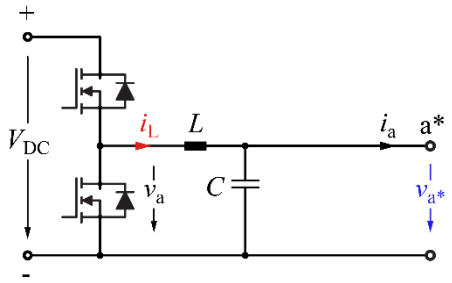
$C_0 = 2nF > C_M$
$R_0 = 4\,\Omega$

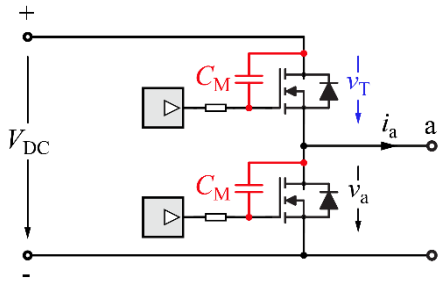
- *$Z_{F,DM}$ Higher Compared to $Z_{F,CM}$ → More Critical*
- *Low Z_F / Large Filter Capacitor → High Losses → Select $Z_{F,DM}$ Only Slightly Below $Z_{M,a^*\text{-}b^*c}$*

Comparison of dv/dt-Filtering Techniques 1/2

- **Passive Concept**
  1. LCR-Filter
  2. Clamped LC-Filter
- **Hybrid Concept ($3f_{sw}$)**
  1. LC-Filter
  2. Multi-Step Switching
- **Active Concept**
  1. Miller Capacitor
  2. Gate Current Control

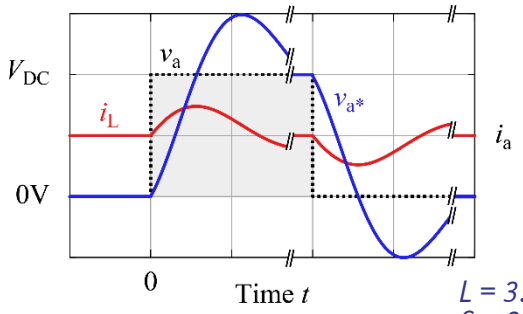




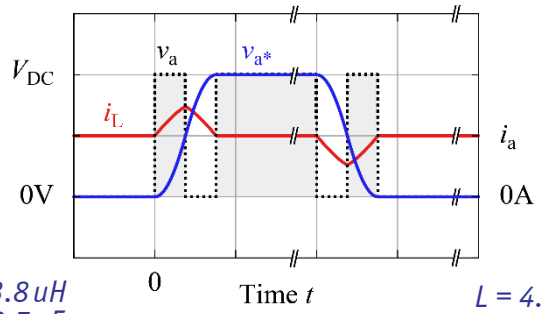


- **Output Voltage Waveforms — V_{DC} = 800V, P_{out} = 10kW, 6kV/us**

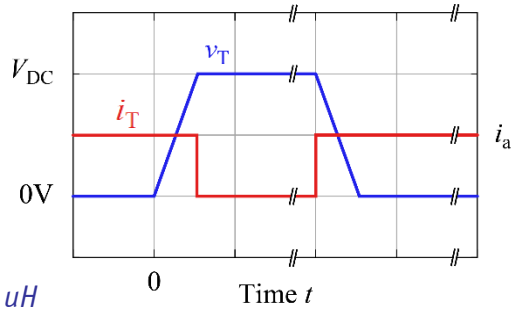
1200V SiC / 16 mΩ
C_M = 120 pF



L = 3.8 uH
C = 2.7 nF
R = 19 Ω

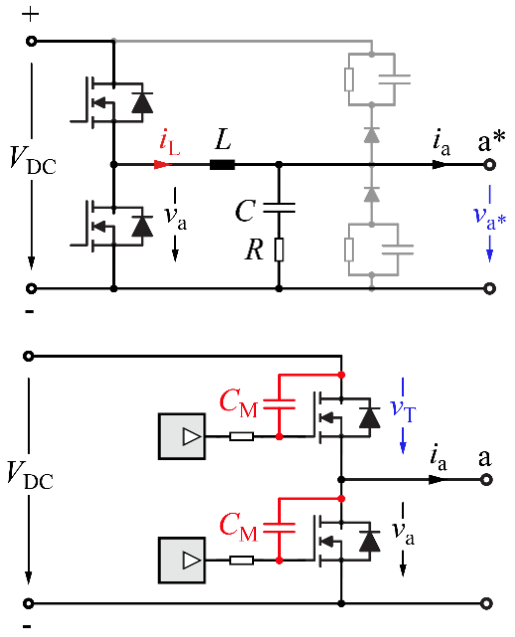


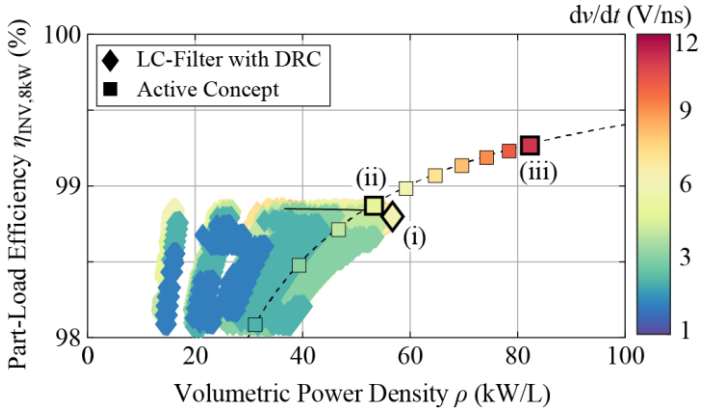
L = 4.1 uH
C = 1.3 nF

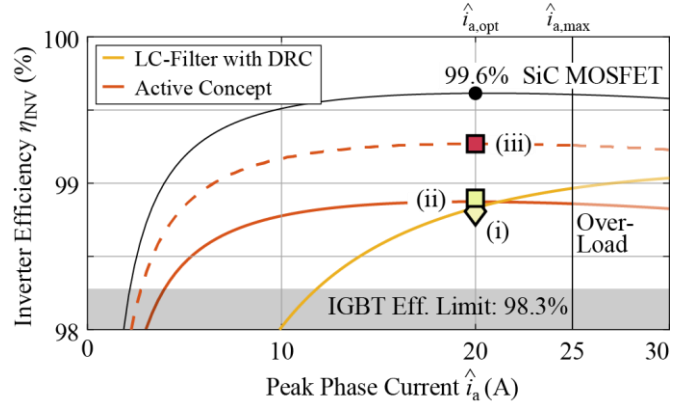


Comparison of dv/dt-Filtering Techniques 2/2

- *Comparative Evaluation of Passive & Active Concept*



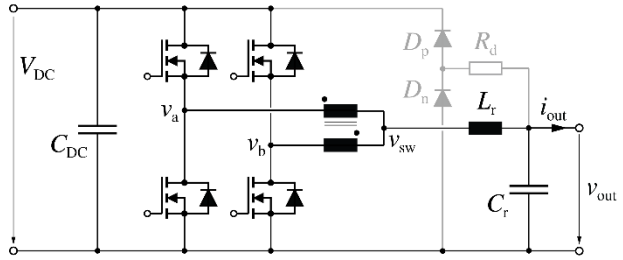


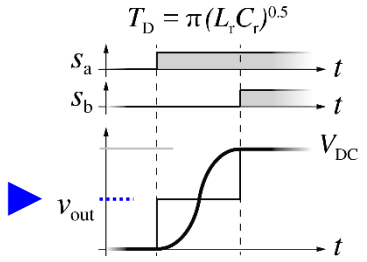


- *Losses / Power Density – V_{DC} = 800V, P_{out} = 10kW, f_{sw} = 16kHz, 1200V SiC-MOSFETs (16mΩ)*

Multi-Bridge-Leg dv/dt-Limitation

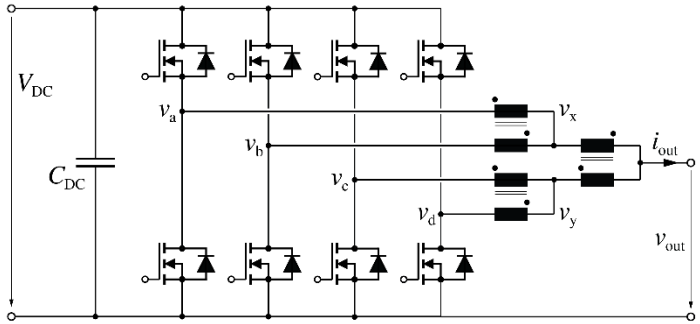
- *2-Step Switching / Resonant Transition (cf. Active dv/dt-Filter)*

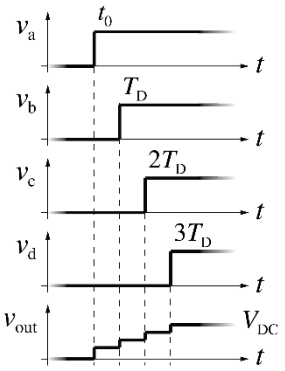




Source: J. Ertl et al. PCIM Europe 2018

- *Staggered Sw. Parallel Bridge-Legs → Non-Resonant Multi-Step Transition*



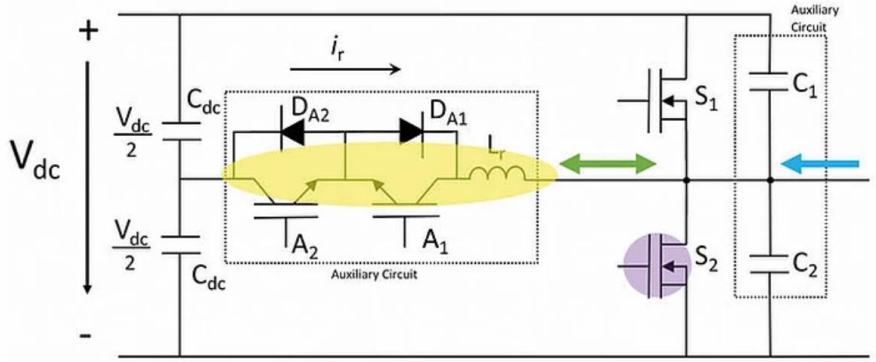


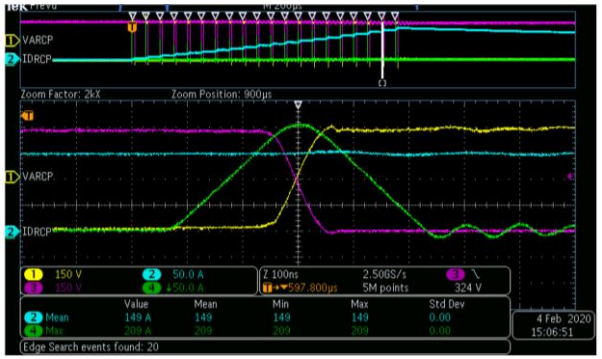
Source: J. Ertl et al. PCIM Europe 2017

- *Adv. for High Power / High Output Curr. Syst. Employing Parallel Bridge-Legs & Local Comm. Caps*

Aux. Resonant Commutated Pole

- *dv/dt-Limitation & Sw. Loss Red. w/ Snubber Cap. & Aux. Switches → 1 ... 1.5 kV/us*
- *Opt. Timing of Aux. & Main Switches → Pre-Flex™ Self-Learning AI Algorithm*
- *Concept Proposed for BJTs by M. Lockwood & A. Fox @ IPEC 1983 (!)*





Pre-Switch, Inc.
We take the hard out of switching.

Green: Lr Resonant inductor current (varies with load)

Purple: S2 Vds switch voltage (600V-0V)

Yellow: Aux + Lr ARCP and inductor voltage (-300V to +300V)

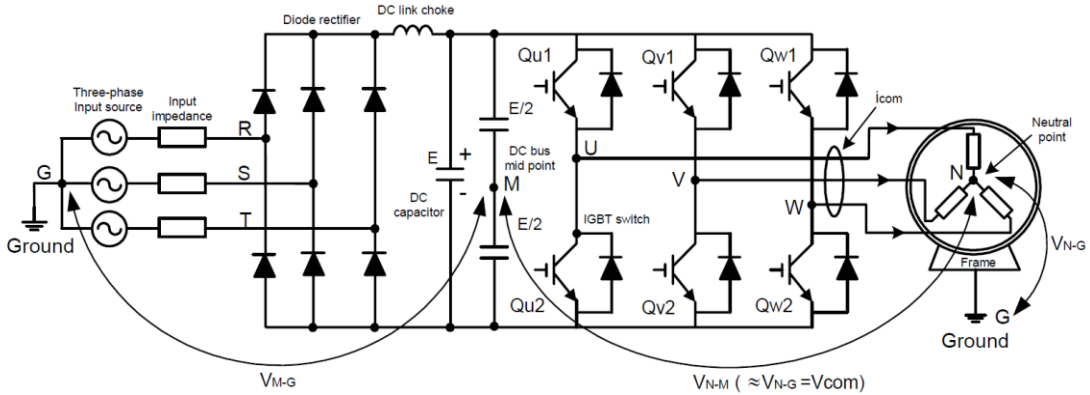
Blue: Load current varies 0-160A

- *Complicated Implementation / Critical Timing for f_{sw} > 100 kHz*
- *99.5% Half-Load | 99.35% Full-Load Eff. @ 100 kW, 800 V_{DC}, f_{sw} = 50 kHz (1200V/12 mΩ SiC MOSFETs)*

Inverter Systems w/ Sinusoidal Output Voltages

Inverter DM & CM Output Filter

- *Measures Ensuring EMI Compliance / Longevity of Motor Insulation & Bearings*
- *Series Reactor | dv/dt-Filter | DM-Sinus Filter | Full-Sinus Filter | Multi-Level Inverter*

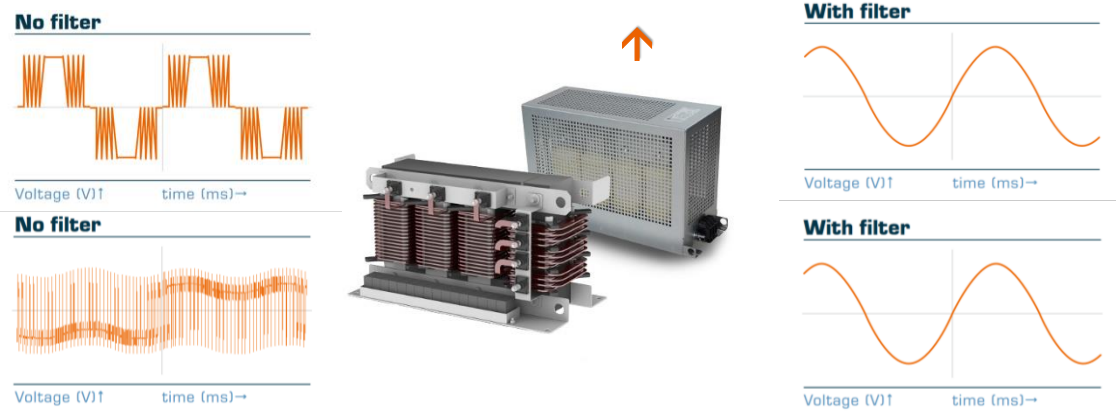


Source: YASKAWA

Source: BLOCK

MOTOR VOLTAGE PHASE-PHASE

MOTOR VOLTAGE PHASE-GROUND

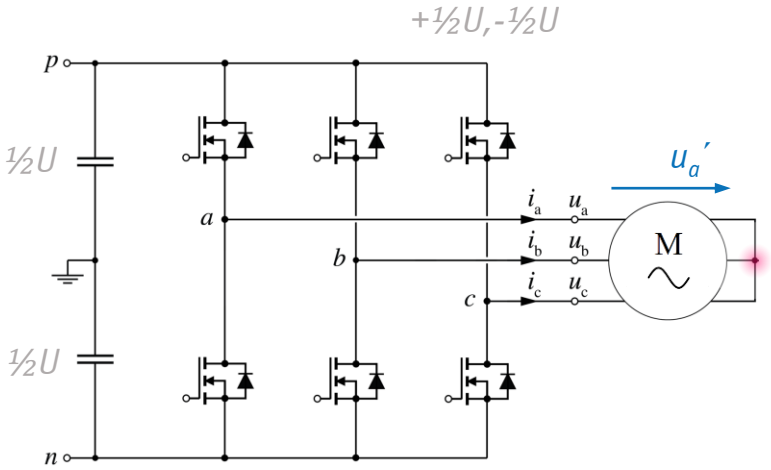


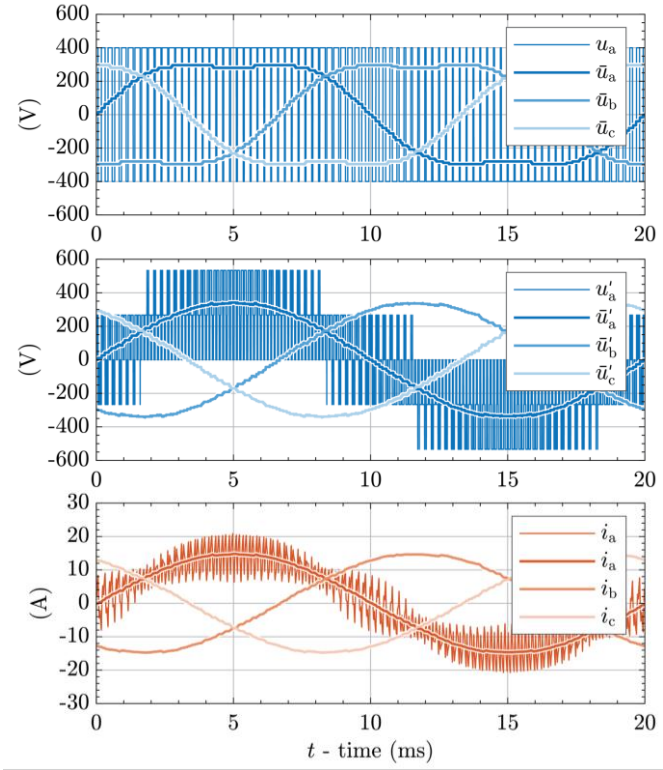
- *Small Filter Size →*
  High Sw. Frequ. → SiC | GaN

Inverter DM & CM Output Voltage Components

2-Level Inverter

- *Open Motor Starpoint → Single Bridge-Leg / Phase*
- *AC Phase Voltage $\hat{U}_{phase}$ Formation Against DC Midpoint*
- *DC Voltage / Blocking Voltage $U_{DC} \approx 2\hat{U}_{phase}$*



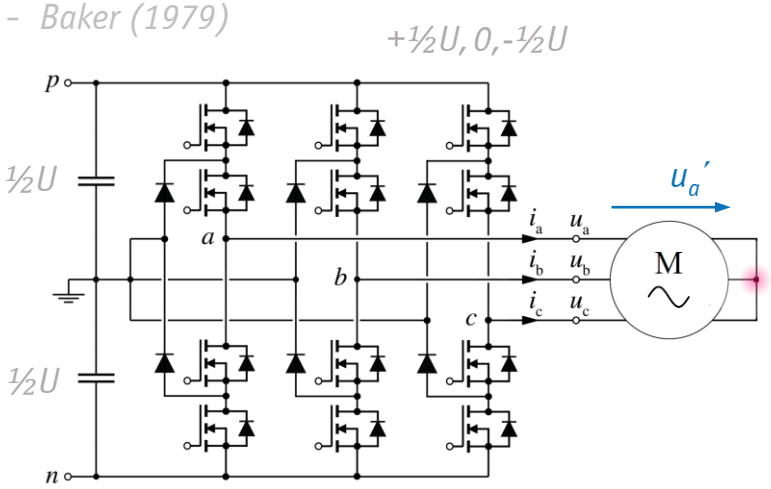


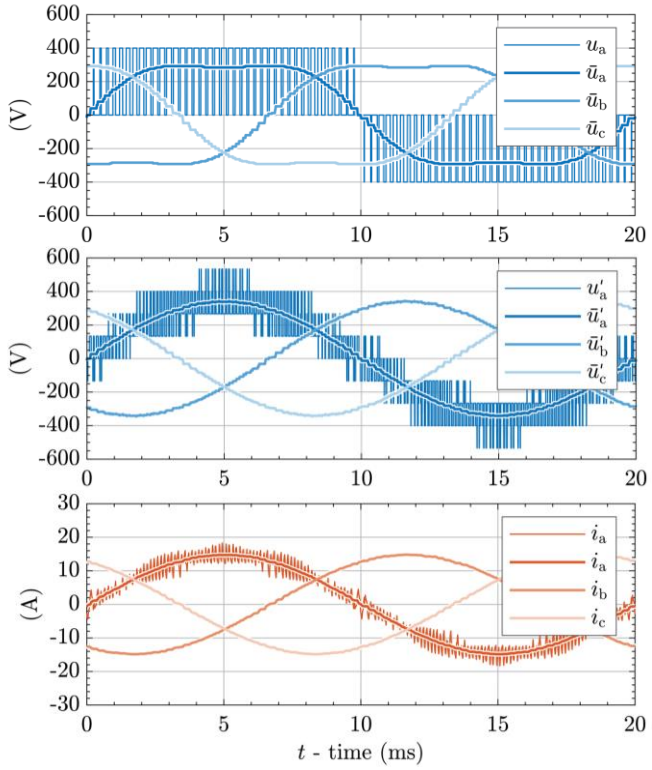
- *Large Sw. Voltage Steps → Rel. High Sw. Losses / Curr. Harmonics / EMI*

3-Level Inverter

- *Neutral Point Clamped (NPC) Topology Features Connection to Cap. DC Midpoint*
- *Larger Number of Sw. States / Higher Output Voltage Quality*
- *Requires Neutral Point Balancing*
- *Blocking Voltage ½U_{DC} ≈ $\hat{U}_{phase}$*

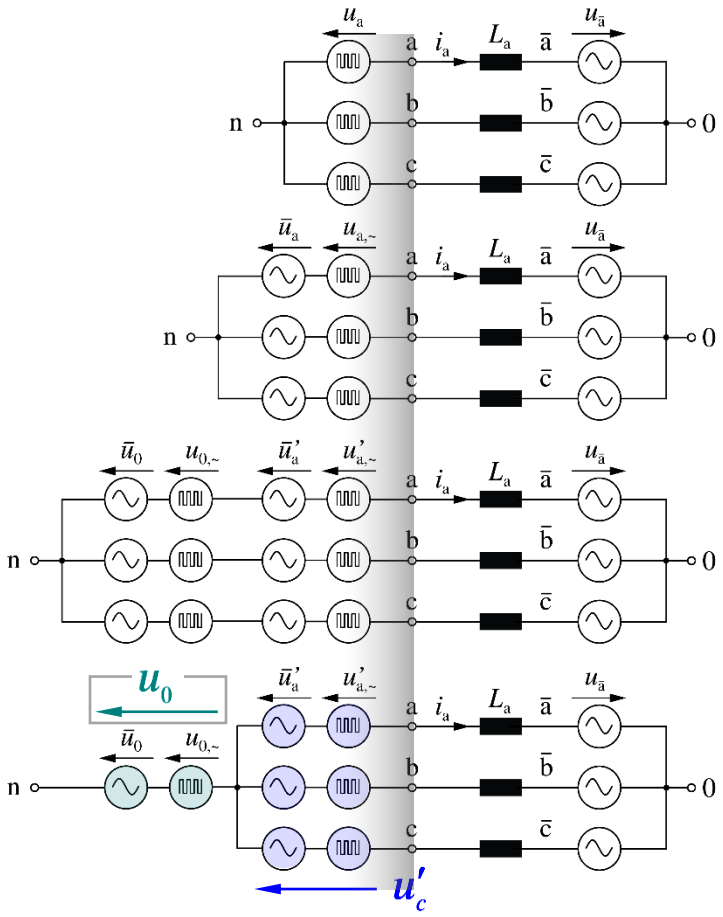
- *Baker (1979)*





- *Rel. High Conduction Losses (T-Type Topology as Alternative)*

Equivalent Circuit 1/3



$$u_a = \bar{u}_a + u_{a\sim}$$
$$u_b = \bar{u}_b + u_{b\sim}$$
$$u_c = \bar{u}_c + u_{c\sim}$$

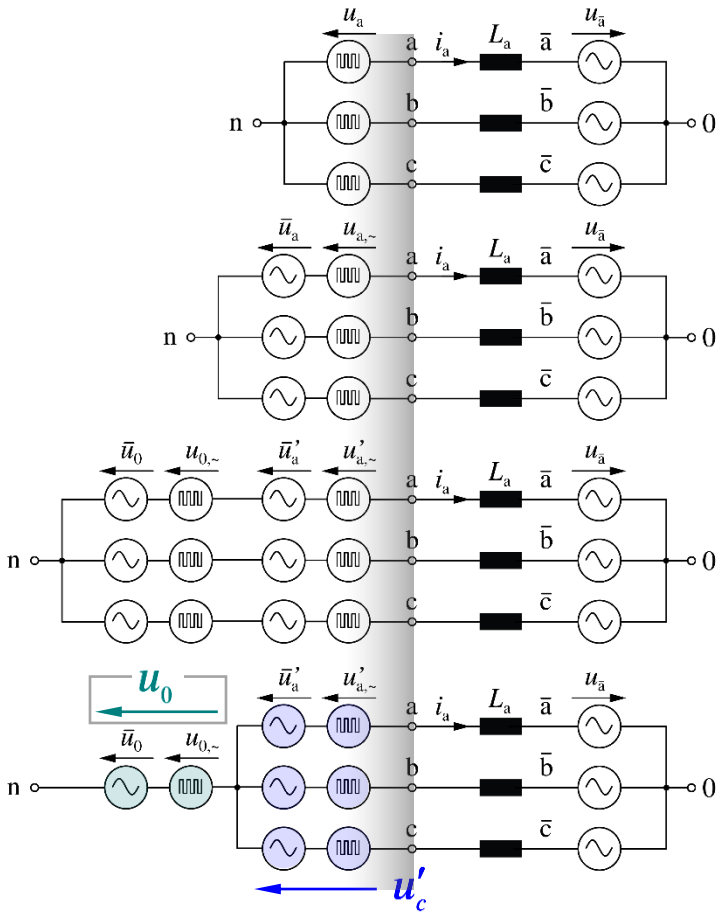
$$u_a = u_a' + u_0 \qquad u_a' + u_b' + u_c' = 0$$
$$u_b = u_b' + u_0$$
$$u_c = u_c' + u_0$$

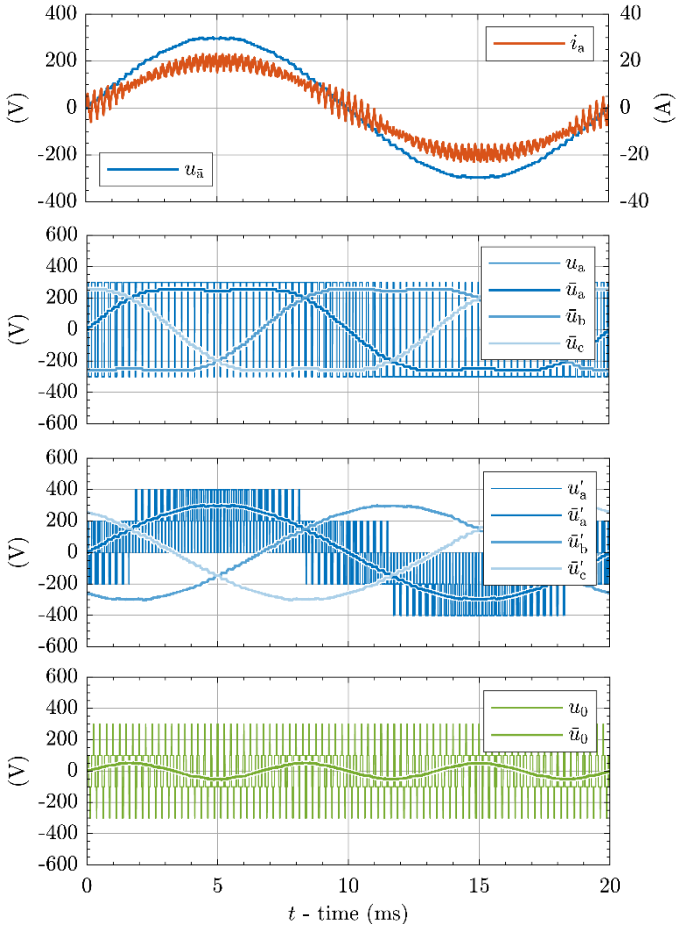
$$u_0 = \tfrac{1}{3}(u_a + u_b + u_c)$$

$$u_a = \bar{u}_a + u_{a\sim}$$
$$u_0 = \bar{u}_0 + u_{0\sim}$$

- *Active DM Voltage Component* u_c'
- *Inactive CM Zero-Sequence Voltage* u_0
- *Low-Frequ. & Sw.-Frequ. Components*

Equivalent Circuit 2/3



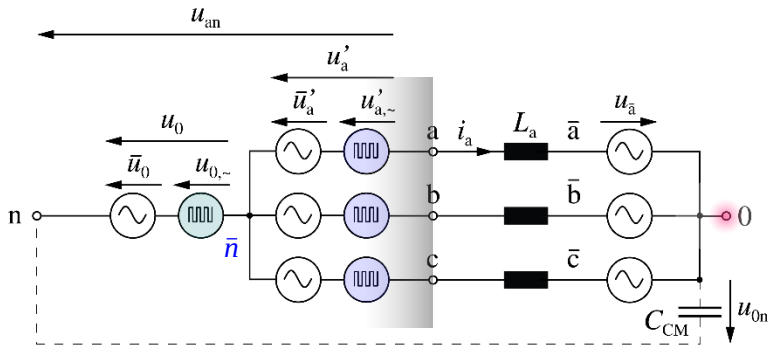


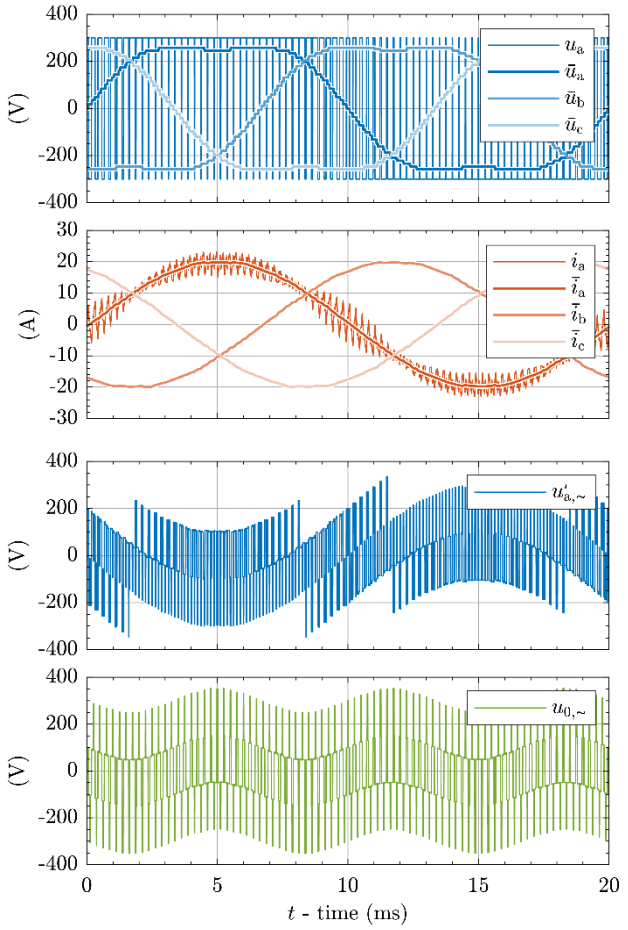
Equivalent Circuit 3/3

- *Active Sw.-Frequ. DM Voltage*
- *Inactive Sw.-Frequ. CM Voltage*

$$u_0 = u_{0n} \quad \rightarrow \quad u_{\bar{n}0} \equiv 0$$

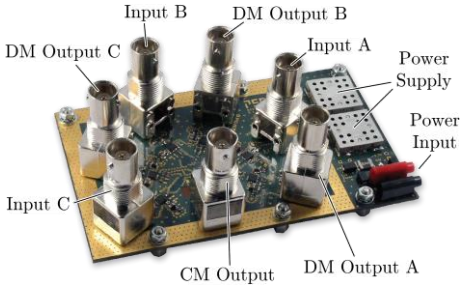
$$\begin{aligned} u_0 + u'_a &= L\frac{di_a}{dt} + u_a + u_{0n} \\ u_0 + u'_b &= L\frac{di_b}{dt} + u_b + u_{0n} \\ u_0 + u'_c &= L\frac{di_c}{dt} + u_c + u_{0n} \\ \hline 3u_0 + 0 &= \quad 0 \quad + 0 \quad + 3u_{0n} \end{aligned}$$

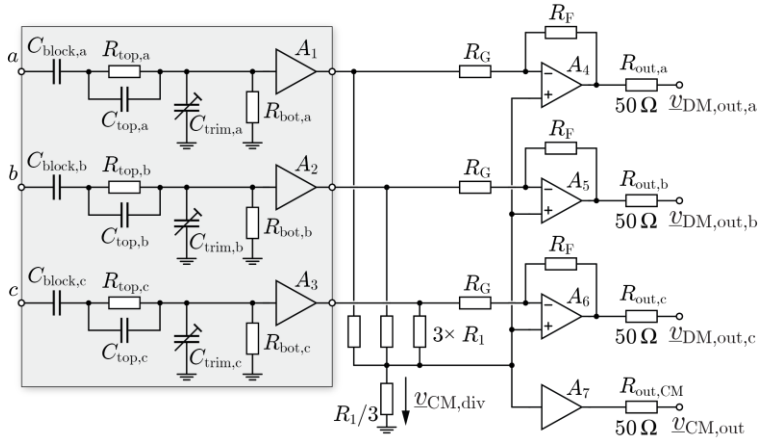


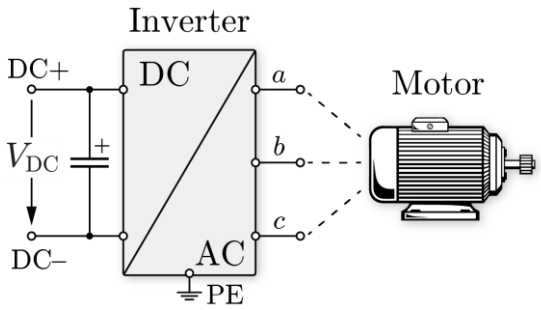


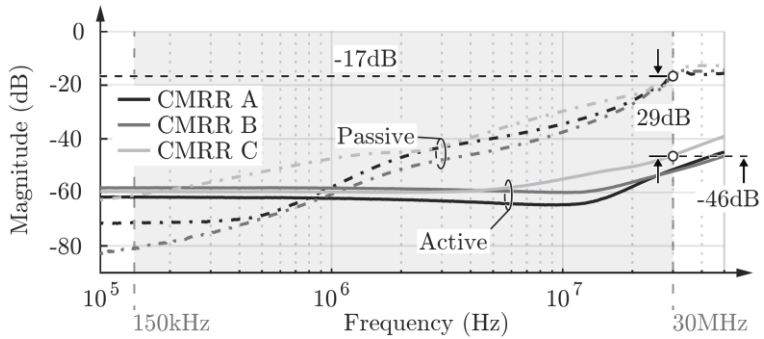
Remark 3-Φ DM/CM EMI Separation

- *EMI Measurement @ Inverter Output*
- *DM/CM Splitting for Specific Filter Design*





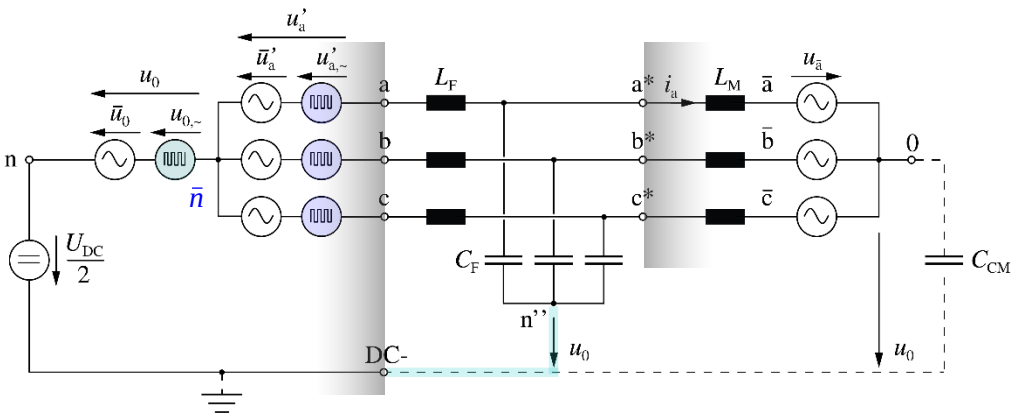


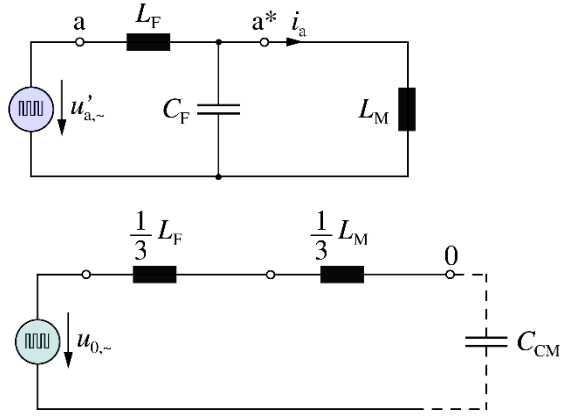


- *Cap. Coupled Interface Circuit as Replacement for LISN (Var. Output Frequ.)*

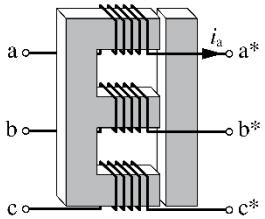
DM/CM Output Voltage Filtering

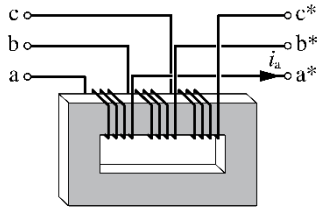
DM & CM Equivalent Circuit

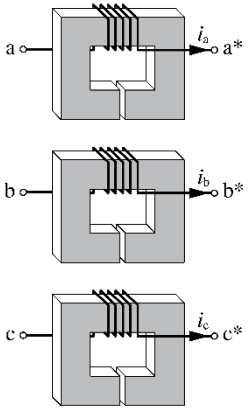




Filter Inductor Types





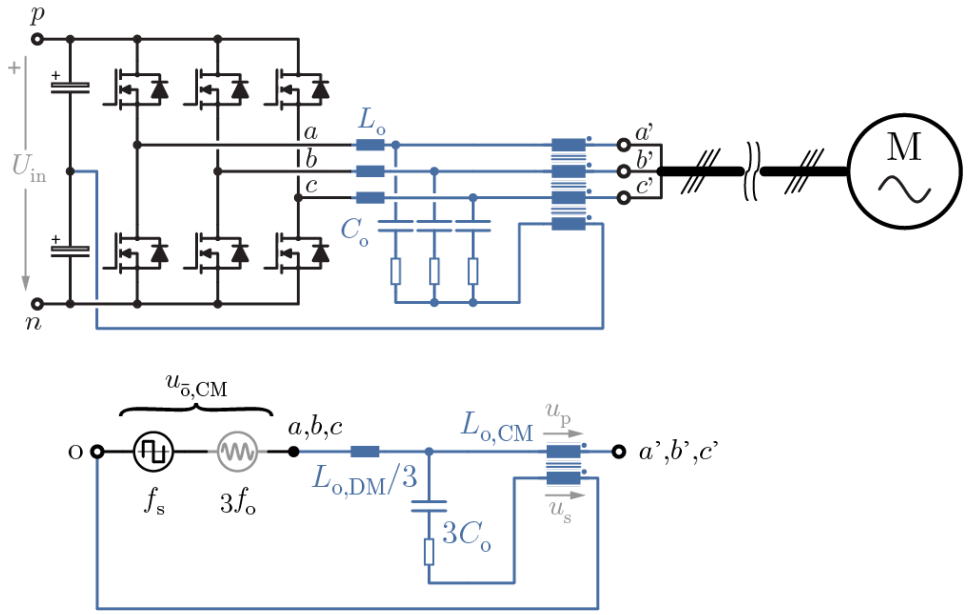


- DM Inductor / CM Inductor / Phase Inductors

Active CM-Voltage Filtering

Active CM Voltage Filters 1/2

- *Series Compensation of CM-Voltage & DM dv/dt-Filtering*

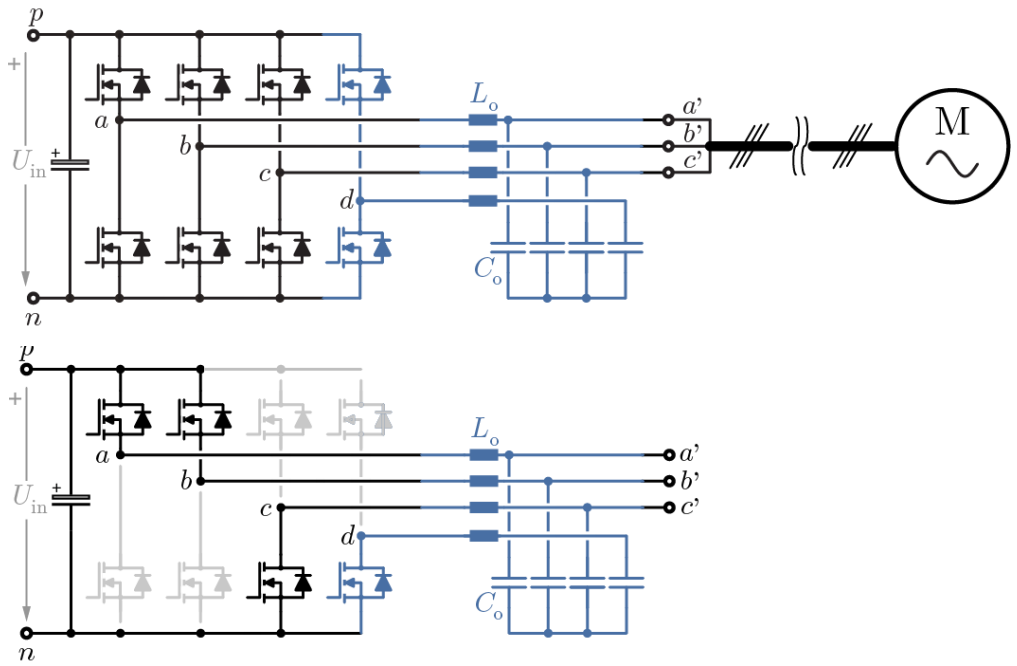


Source: X. Chen et al., 2007

- *Residual CM-Volt. Due to CM-Transf. & Sw. Imperfections / Complexity*

Active CM Voltage Filters 2/2

- *Aux. Bridge-Leg → Zero CM-Voltage for Active Inv. Sw. States & DM dv/dt-Filtering*



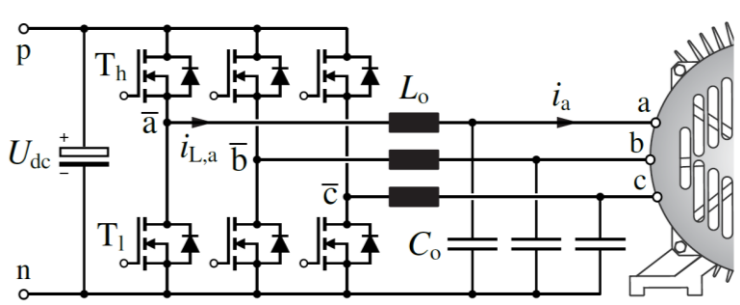
Source: T.A. Lipo et al., 1999

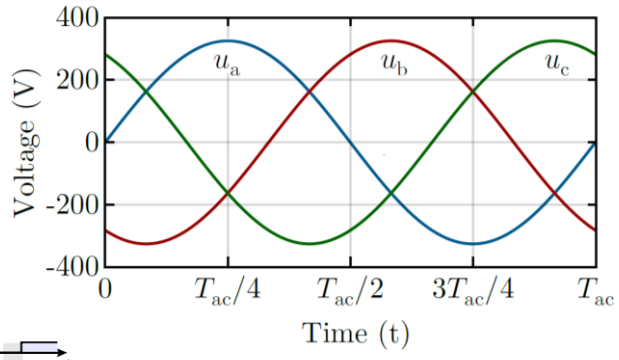
- *Residual CM-Volt. Due to CM-Transf. & Sw. Imperfections / Complexity & Missing Zero State*

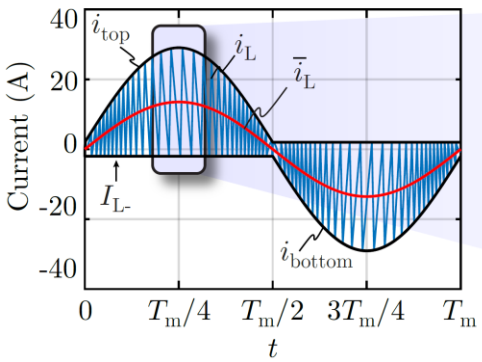
Sinusoidal Output
Triangular Current Mode (TCM)
ZVS Operation

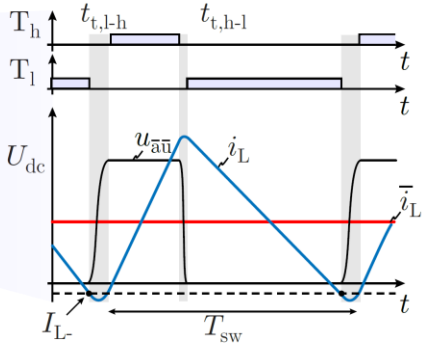
Full-Sinewave Filter & ZVS Operation

- *Purely Sinusoidal Output Voltage (DM & CM Filtering)*
- *High Sw. Frequency & TCM → Low Filter Inductor Volume*
- *ZVS of Inverter Bridge-Legs*







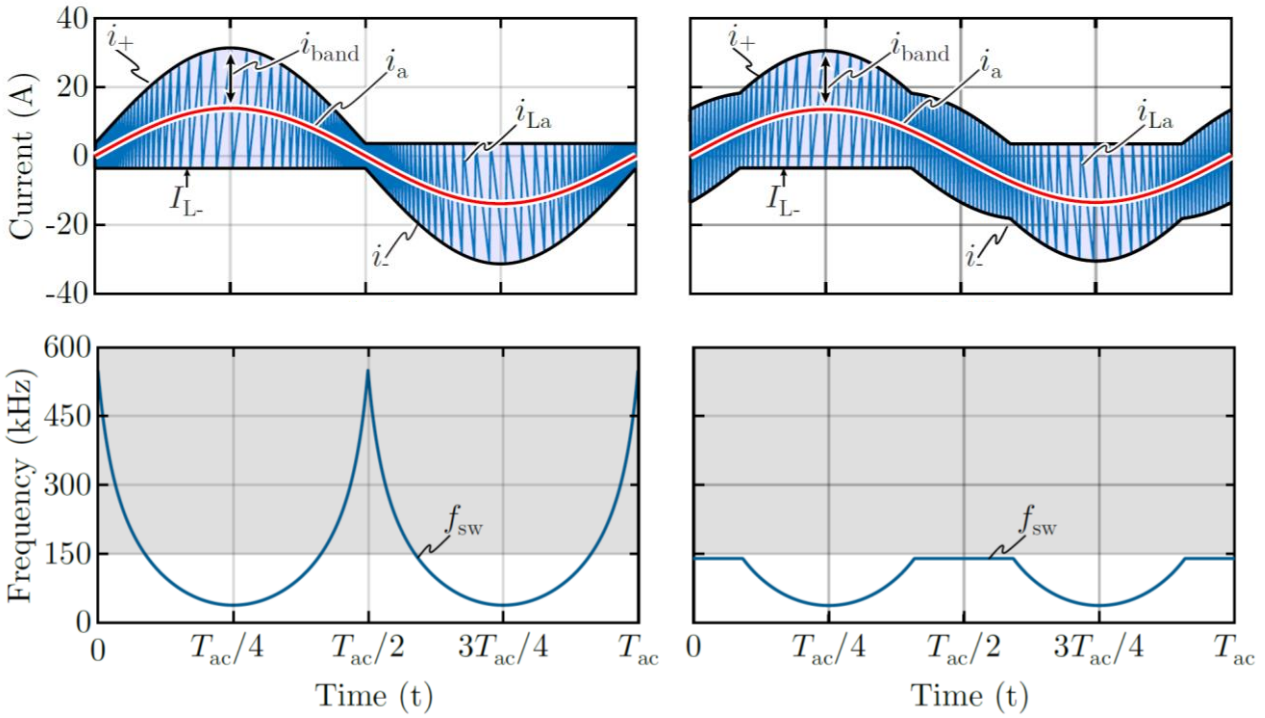


NFO Sinus

- *Only 33% Increase of Transistor Conduction Losses Compared to CCM (!)*
- *Very Wide Switching Frequency Variation*

Frequency-Bounded TCM → B-TCM

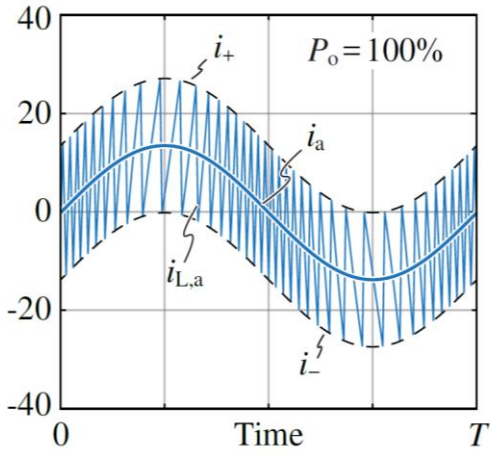
- *Very Wide Switching Frequency Variation of TCM → B-TCM*

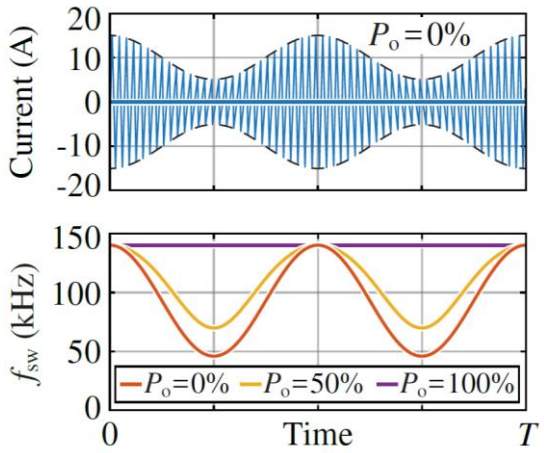


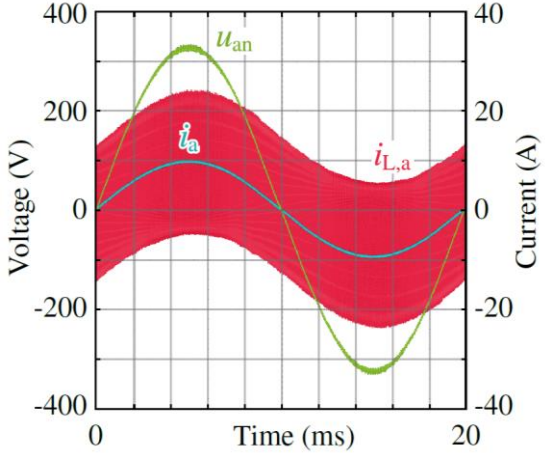
- *TCM → B-TCM — 10% Further Increase of Transistor Conduction Losses*

Frequency-Bounded B-TCM → S-TCM

- *Sinusoidal Switching Boundaries → S-TCM*
- *Adaption for Low Output Power Considering $f_{sw,max}$= 140kHz*





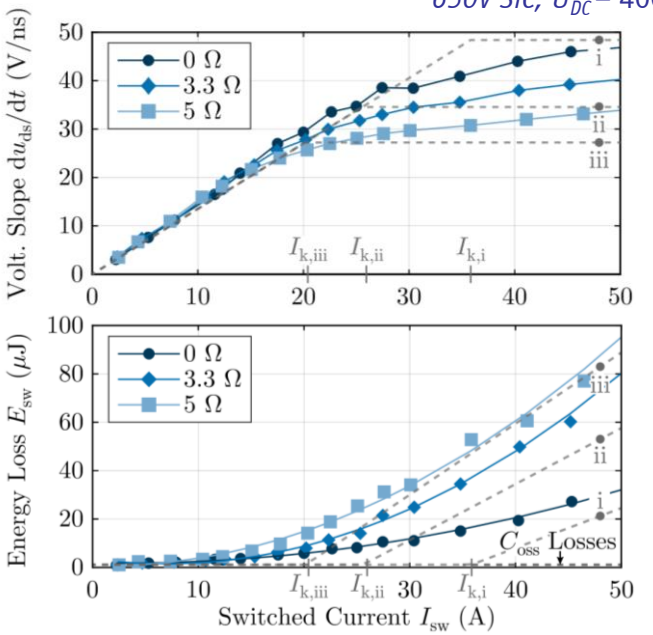


- *TCM → S-TCM ≈ 10% Further Increase of Transistor Conduction Losses*

Remark Residual ZVS Losses

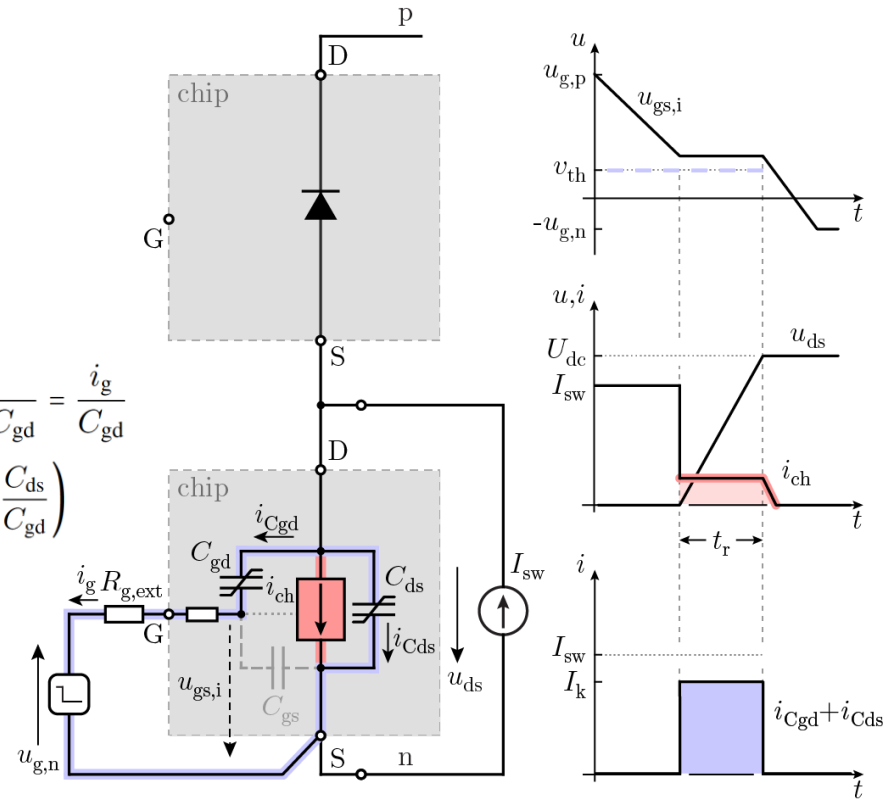
- *Overlap of u_{DS} & Channel Current i_{ch} @ High $I_{sw} > I_k$*
- *Temporary Turn-on Due to $u_{GS,i} > u_{th}$*

650V SiC, U_{DC} = 400V



$$\left.\frac{\mathrm{d}u_{ds}}{\mathrm{d}t}\right|_{max} = \frac{I_k}{C_{ds}+C_{gd}} = \frac{i_g}{C_{gd}}$$

$$I_k = \frac{u_{th}+u_{g,n}}{R_g}\left(1+\frac{C_{ds}}{C_{gd}}\right)$$



- *"Kink" Current I_K Dependent on Inner & Outer Gate Resistance & $u_{g,n}$*

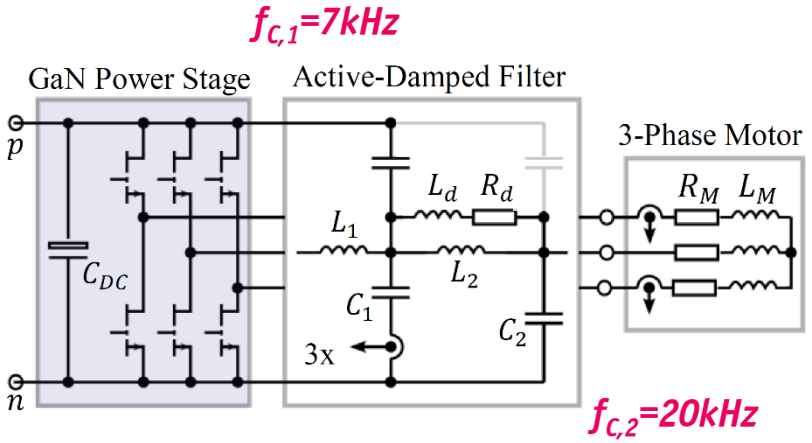
Sinusoidal Output Continuous Current Mode (CCM) Operation

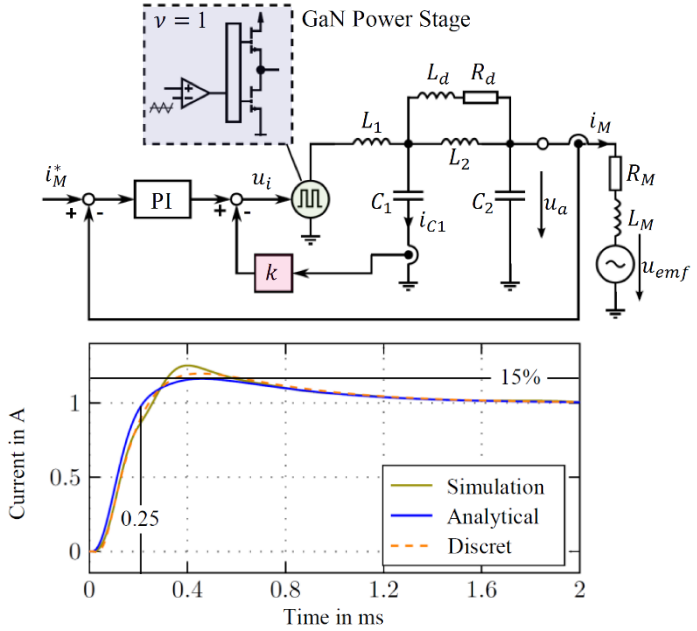
Full-Sinewave 2-Stage Output Filter 1/3

PERFECTION IN AUTOMATION
A MEMBER OF THE ABB GROUP

TECHNISCHE UNIVERSITÄT WIEN
Vienna | Austria

- *Sinewave Output & IEC/EN 55011 Class-A*
- *Low-Loss Active Damping of 1st Filter Stage — Neg. Cap. Current Feedback*
- *2kW / 400V DC-Link 3-Φ 650V GaN Inverter (I_M=5A), $f_{out,max}$ = 500Hz*
- *Sw. Frequency f_{sw}= 100kHz*

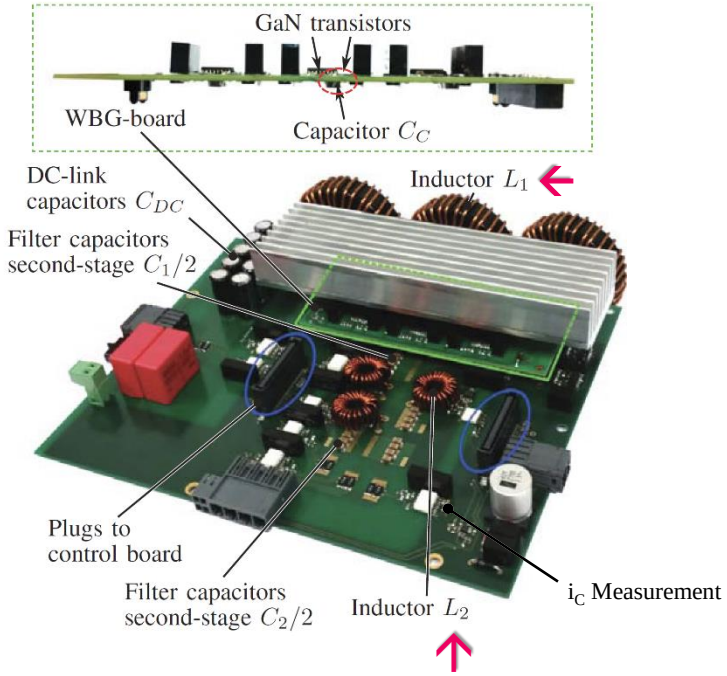


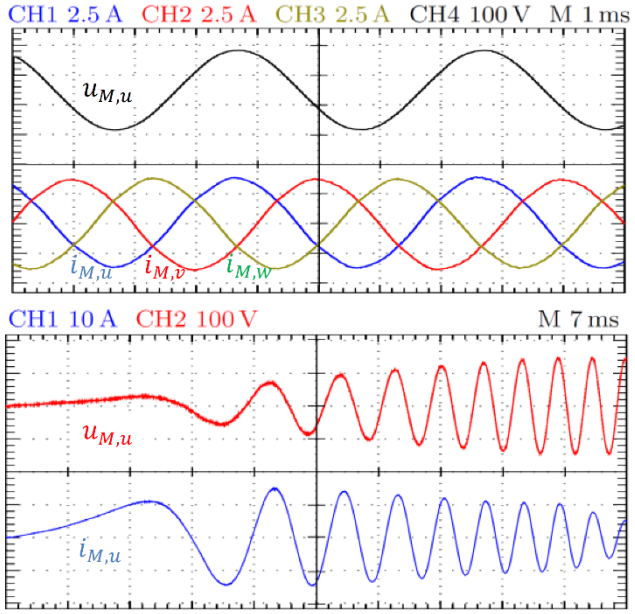


- *Evaluation of Optimized Inductors — Soft Sat. Toroidal Iron Powder Cores*
- *L_1=200uH / C_1=2.5uF | L_2=25uH / C_2=2.5uF / L_d=33uH / R_d=5.6Ω*

Full-Sinewave 2-Stage Output Filter 2/3

- *Exp. Verification — 650V E-Mode GaN Systems Transistors (50mΩ)*
- *Sw. Frequency f_{sw}= 100kHz, Efficiency ≈98%*
- *200mm x 250mm*

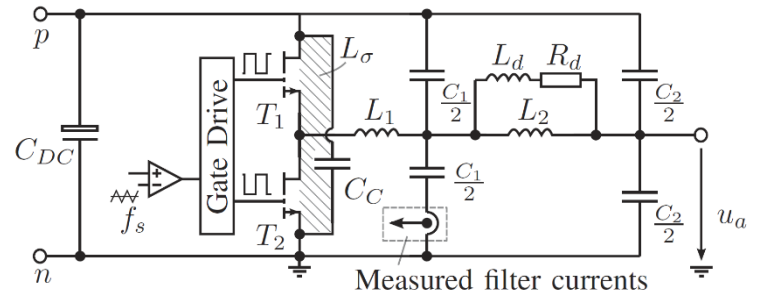


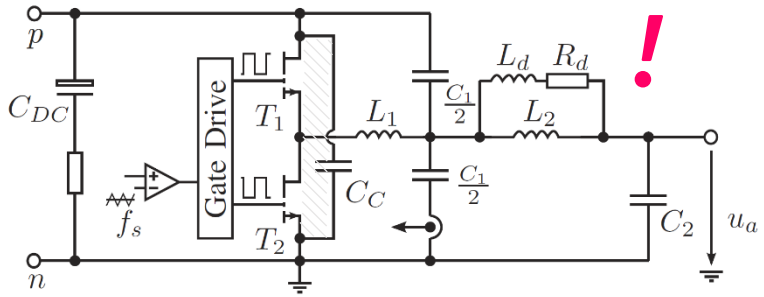


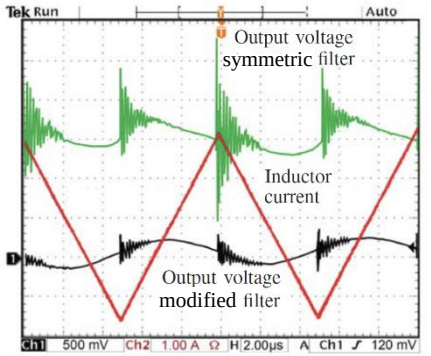
- *Stationary Motor Phase Curr. /Voltage @ 2.5Nm & f_{out}=250Hz*
- *Speed Increase from Standstill to n = 3000rpm in 60ms*

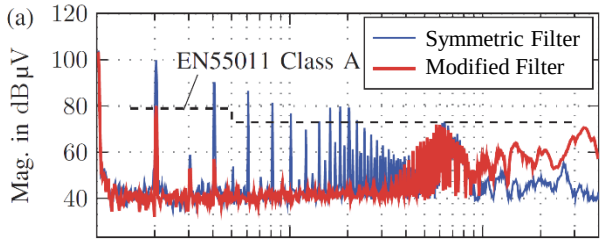
Full-Sinewave 2-Stage Output Filter 3/3

- *Modification of Output Filter Structure*
- *Elimination of Direct Cap. Coupling Between Output and Noisy (!) DC+ (Due to ESR of C_{DC})*
- *For Opt. i_c-Feedback C_1 Realized Using ≈Linear Kemet KC-Link*





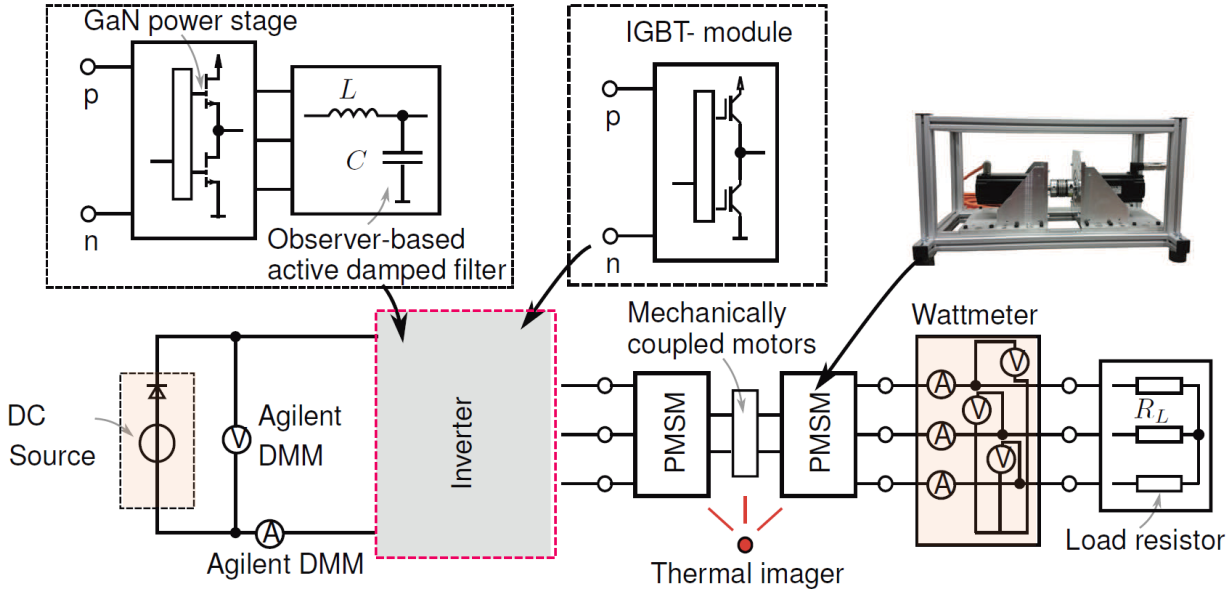


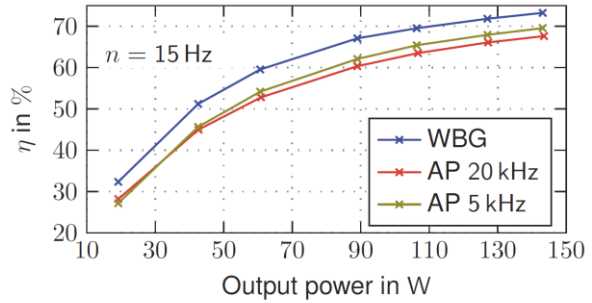


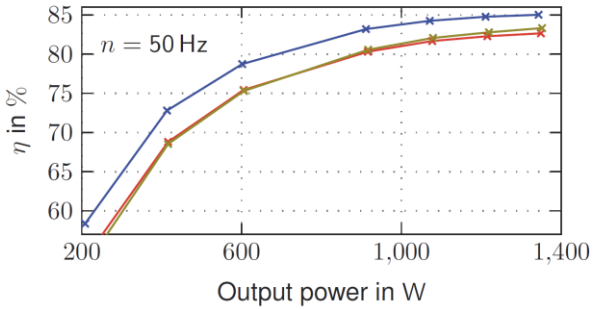
- *Modified Filter → Compliance to EMI Standard EN55011 Class-A*

GaN vs. IGBT Inverter Efficiency Comparison

- *Si Easypack 1200V/35A vs. GaN 650V/30A (50mΩ)*
- *5...20kHz Standard PWM IGBT Motor Inverter (B&R Industrial Automation)*
- *Efficiency Measurement — Inverter DC Input → Load Machine AC Output*





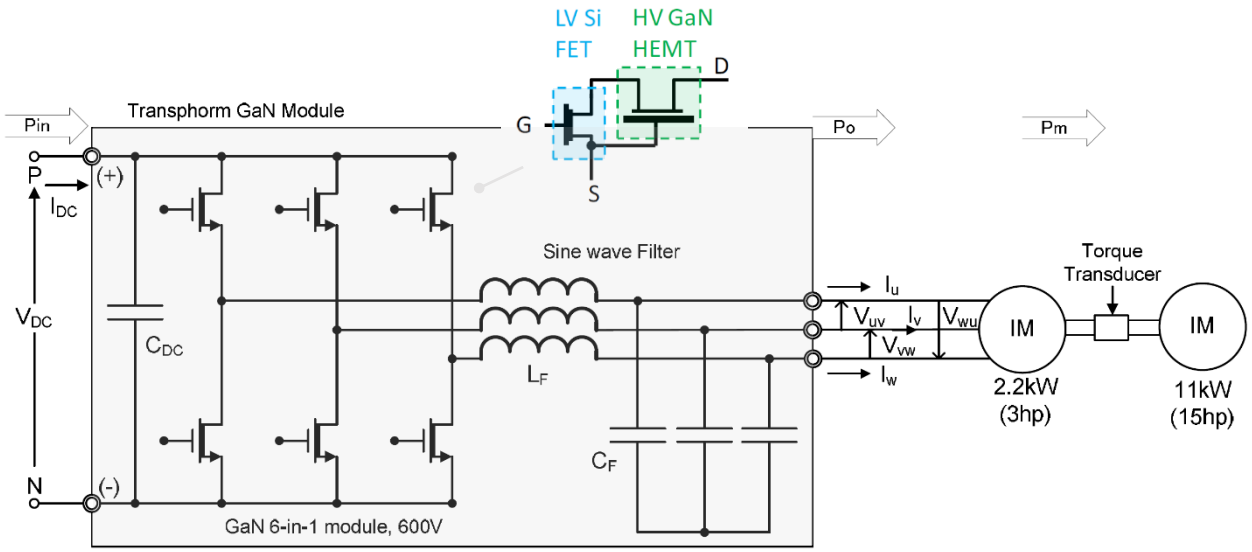


- *Efficiency Improvement of 2-4% in Whole Operating Range*
- *Low Sw. Losses of GaN Inverter & Low Output Filter Losses & Low Motor Iron Losses*

3-Φ 650V GaN Inverter System 1/2

Source: YASKAWA

- *Transphorm 650V Normally-On GaN HEMT/30V Si-MOSFET Cascode 6-in-1 Power Module*
- *Sinewave LC Output Filter — Corner Frequency f_C= 34kHz (f_{sw}= 100kHz)*
- *No Freewheeling Diodes*

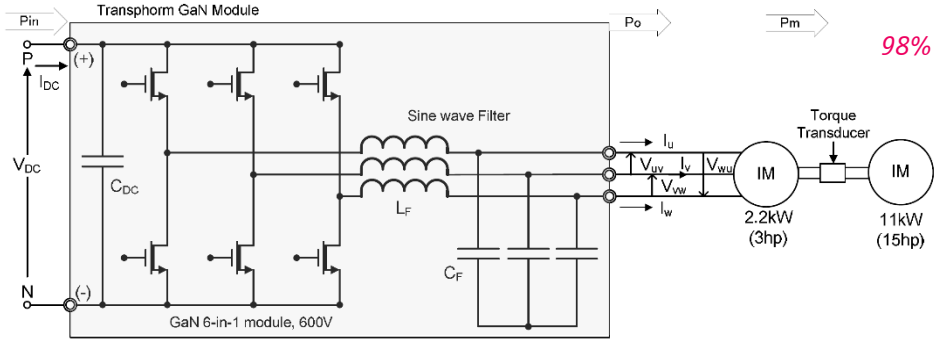


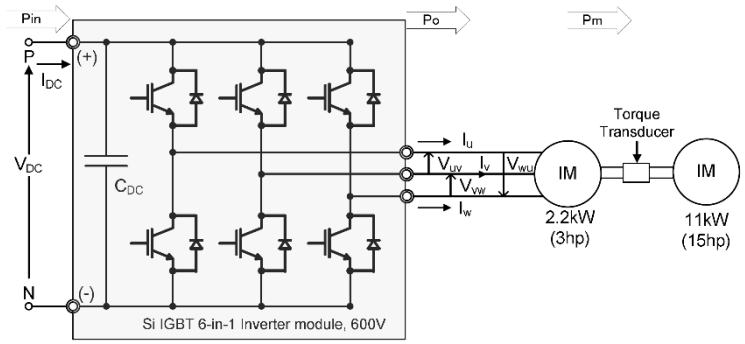
→ *Comparison to Si-IGBT Drive Systems*

3-Φ 650V GaN Inverter System 2/2

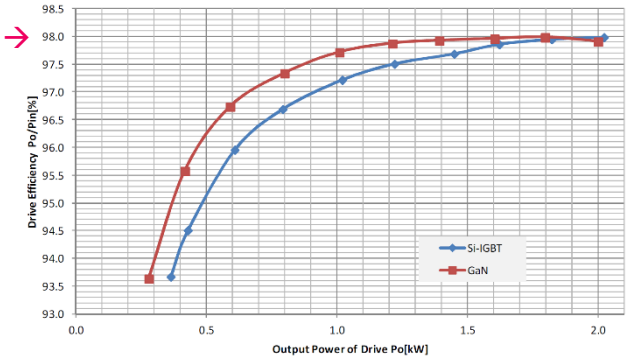
Source: YASKAWA

- *Comparison of GaN Inverter w/ LC-Filter to Si-IGBT System (No Filter, f_{sw}=15 kHz)*
- *Measurement of Inverter Stage & Overall Drive Losses @ 60 Hz*

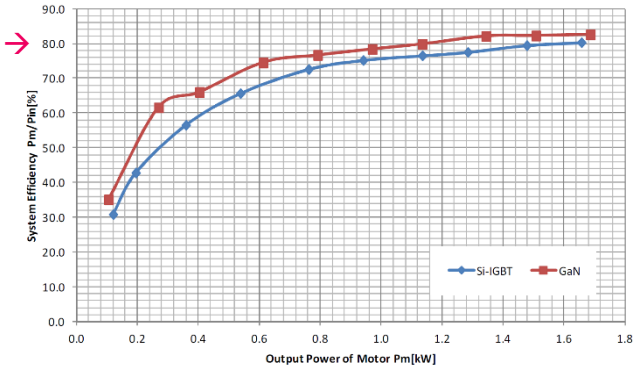




98% →



80% →

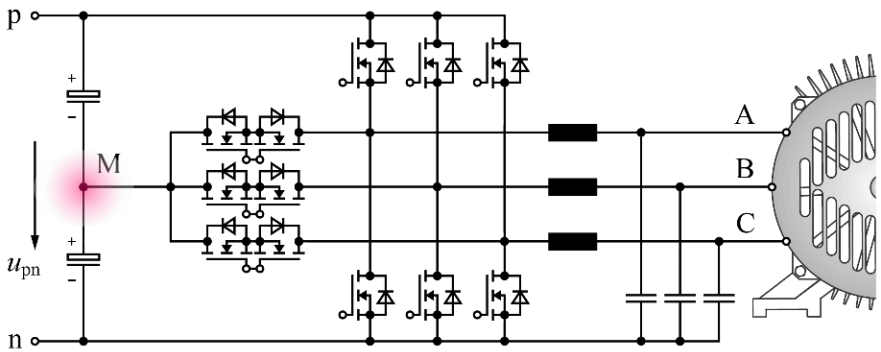


- *2% Higher Efficiency of GaN System Despite LC-Filter (Saving in Motor Losses) !*

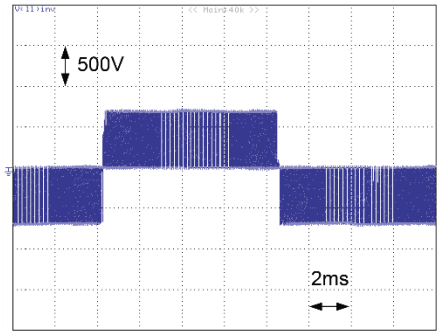
Multi-Level / Multi-Cell Converters & Modularity

3-Level T-Type Inverter 1/3

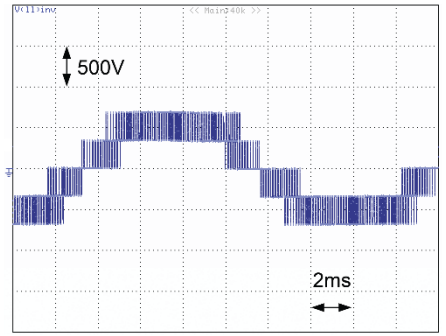
- *Higher Number of Bridge-Leg Output Voltage Levels / Lower DM & CM Voltage Steps*
- *Neutral Point Clamped | Flying Capacitor | T-Type Bridge-Leg Topologies*



Motor Line-to-Line Voltage



2-Level Bridge-Leg

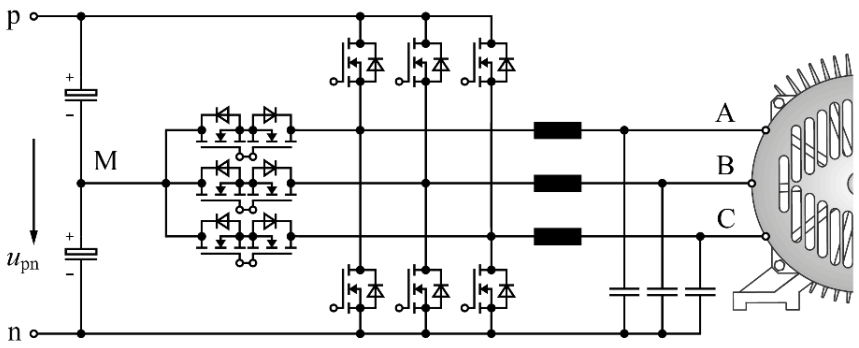


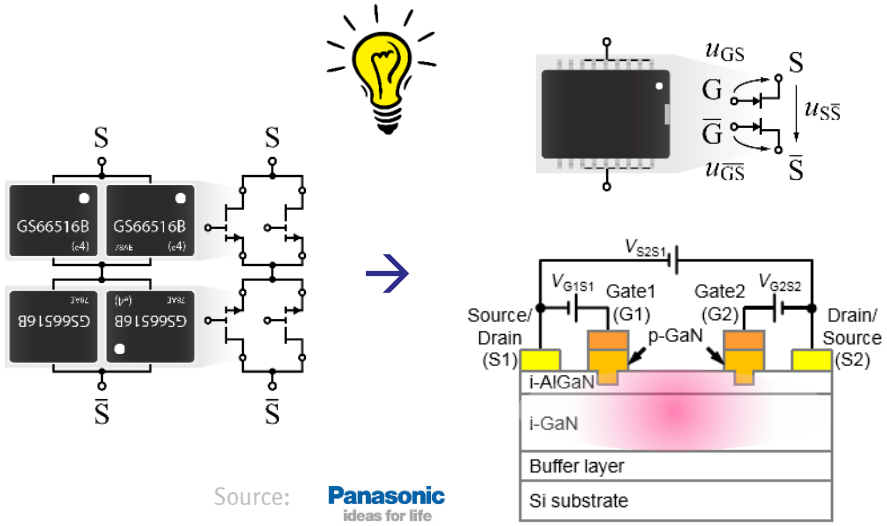
3-Level Bridge-Leg

- *More Complicated Bridge-Leg Structure*
- *On-State-Losses of Series-Connected Switches*

3-Level T-Type Inverter 2/3

- *3-Level T-Type Inverter — 3-Level Phase Voltage / 5-Level Line-to-Line Voltage*
- *Lower DM & CM Voltage Steps Compared to 2-Level Converter*

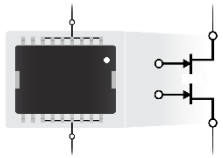


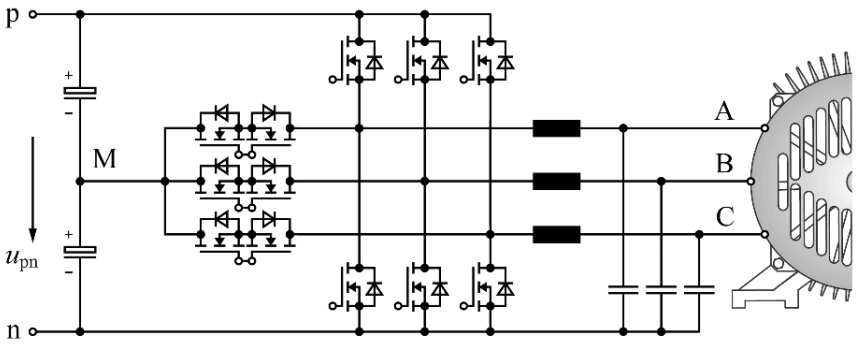


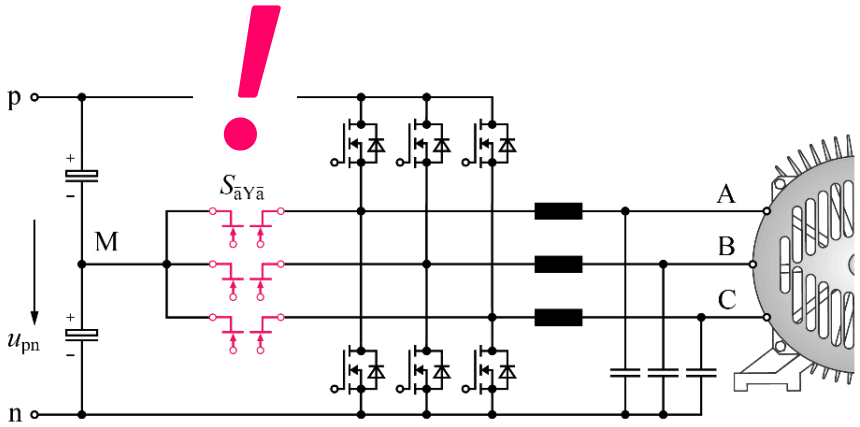
- *Full-Sinewave DC-Link Referenced LC-Filter — Elimination of DM & CM Sw. Frequ. Voltage Harmonics*
- *T-Type Topology Ensures Low Conduction Losses — Adv. Application of M-BDSs (!)*

3-Level T-Type Inverter 3/3

- *3-Level T-Type Inverter — 3-Level Phase Voltage / 5-Level Line-to-Line Voltage*
- *Lower DM & CM Voltage Steps Compared to 2-Level Converter*





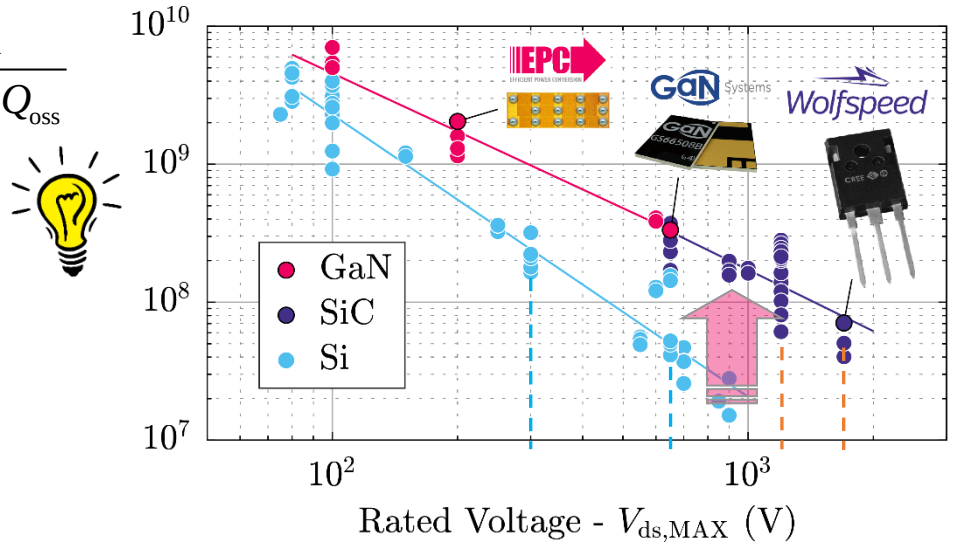


- *Full-Sinewave DC-Link Referenced LC-Filter — Elimination of DM & CM Sw. Frequ. Voltage Harmonics*
- *T-Type Topology Ensures Low Conduction Losses — Adv. Application of M-BDSs (!)*

SiC/GaN Figure-of-Merit

- *Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties*
- *FOM Identifies Max. Achievable Efficiency @ Given Sw. Frequ.*

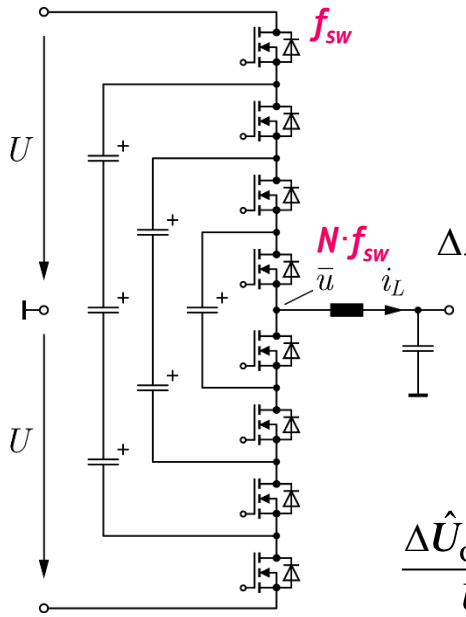
$$\text{FOM} = \frac{1}{R_{\text{ds,on}} Q_{\text{oss}}}$$



- *Advantage of LV over HV Power Semiconductors →*
- *Advantage of Multi-Level over 2-Level Converter Topologies*

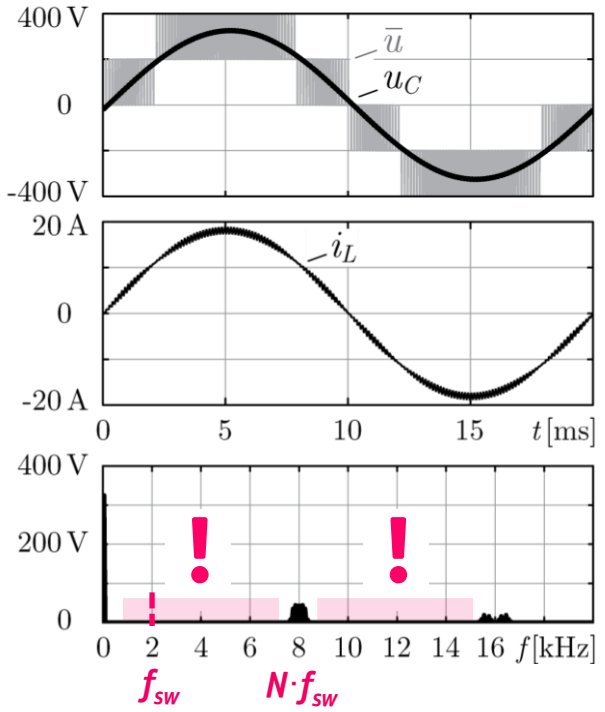
Scaling of Flying Capacitor Multi-Level Concepts

- *Series Interleaving → Reduced Ripple*
- *$f_{sw,eff} = N \cdot f_{sw}$ @ f_{sw}-Determined (!) Switching Losses*
- *Lower Overall On-Resistance @ Given Blocking Voltage*
- *Application of LV Technology @ HV*



$$\Delta\hat{I}_{\max,N} = \frac{1}{N^2}\Delta\hat{I}_{\max,N=1} \quad \Big/ \; \frac{U}{8 f_s L}$$

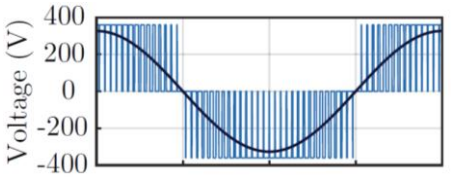
$$\frac{\Delta\hat{U}_{C,\max,N}}{U} = \frac{\pi^2}{32}\left(\frac{f_O}{f_S}\right)^2 \frac{1}{N^3}$$

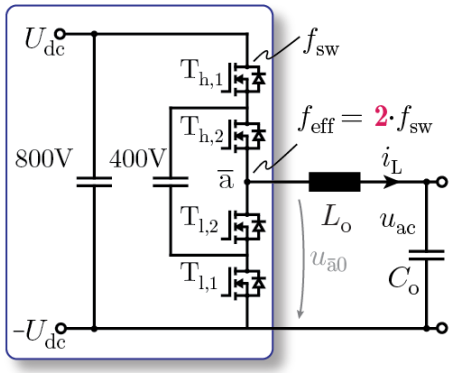


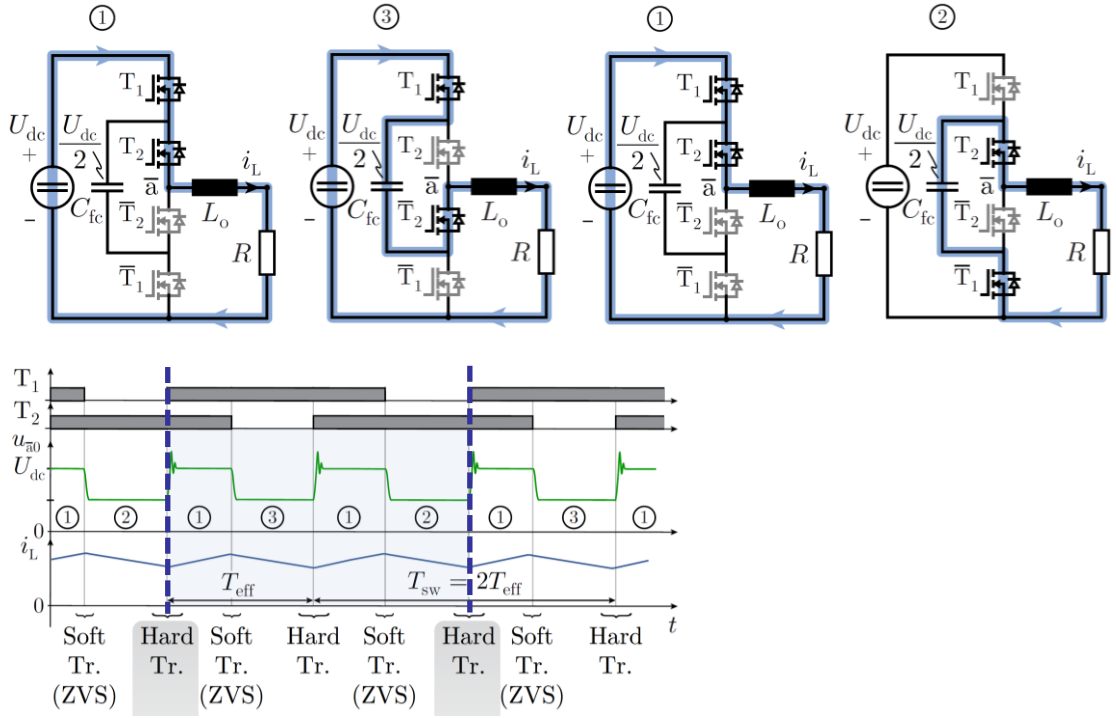
- *Scalability / Manufacturability / Standardization / Redundancy*

3-Level Flying Capacitor (FC) Converter

- *3-Level Flying Cap. (FC) Converter → No Connection to DC-Midpoint*
- *Involves All Switches in Voltage Generation → Eff. Doubles Device Sw. Frequency*





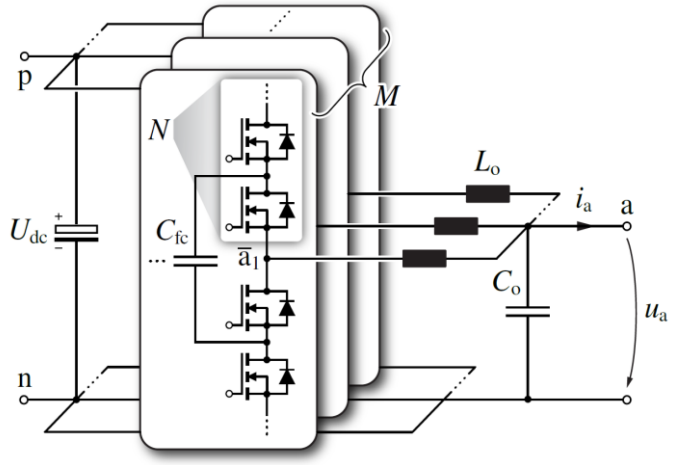


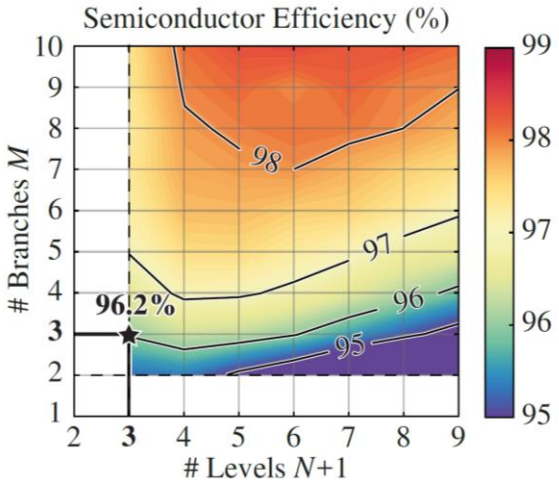
- *FC Voltage Balancing Possible also for DC Output*

4.8MHz GaN Half-Bridge Phase Module

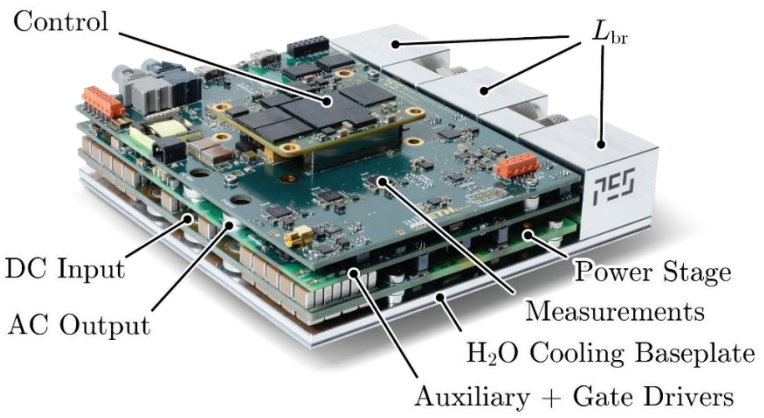
- *Combination of Series & Parallel Interleaving*

— *600V GaN Power Semiconductors, f_{sw}= 800kHz*
— *Volume of ≈180cm³ (incl. Control etc.)*
— *H_2O Cooling Through Baseplate*





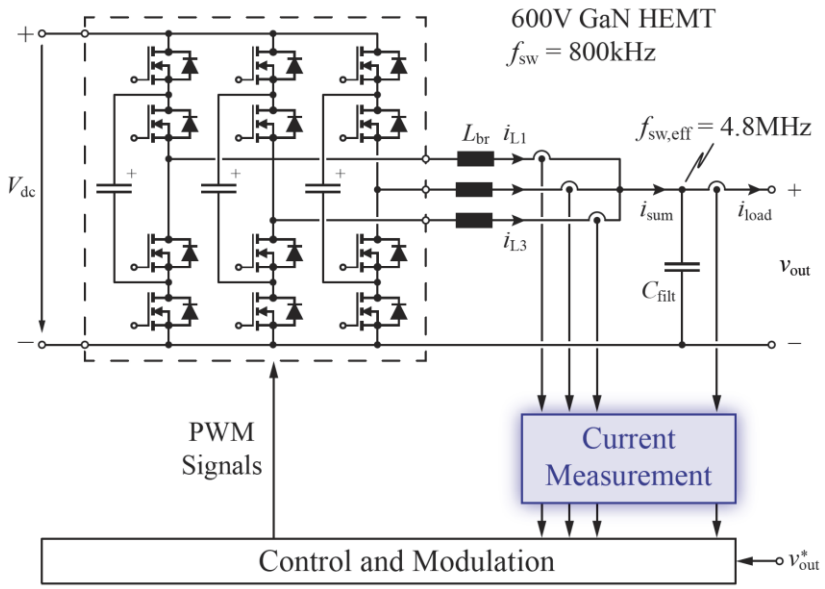
★ *25 kW/dm³*

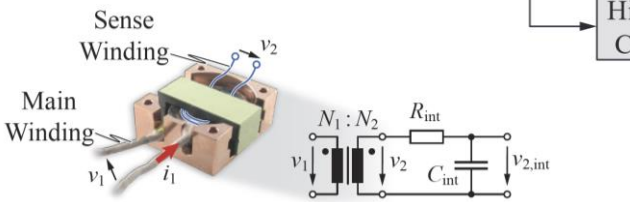


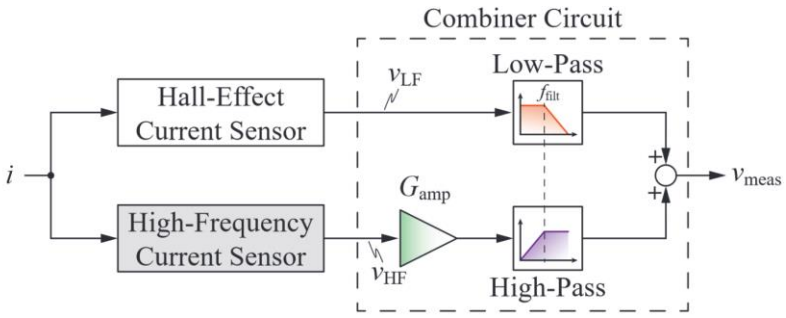
- *Operation @ f_{out}= 100kHz / $f_{sw,eff}$= 4.8MHz, 10kW, U_{dc}= 800V*

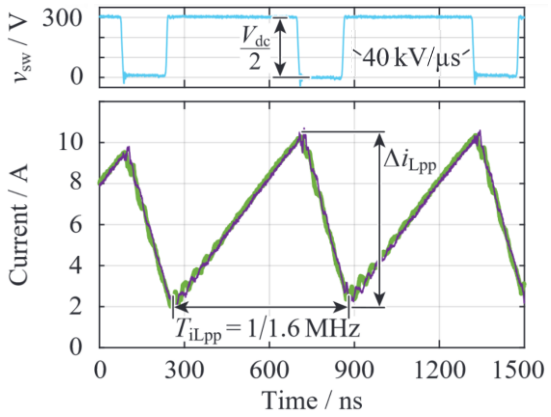
Remark High-BW High-CMRR Current Measurement

- *Extension of Commercial Hall Sensor DC… f_{Hall}≈ 500kHz → DC…10MHz*
- *Low-Pass & High-Pass Filter Network Combining HF-Sensor & LF Hall-Sensor*





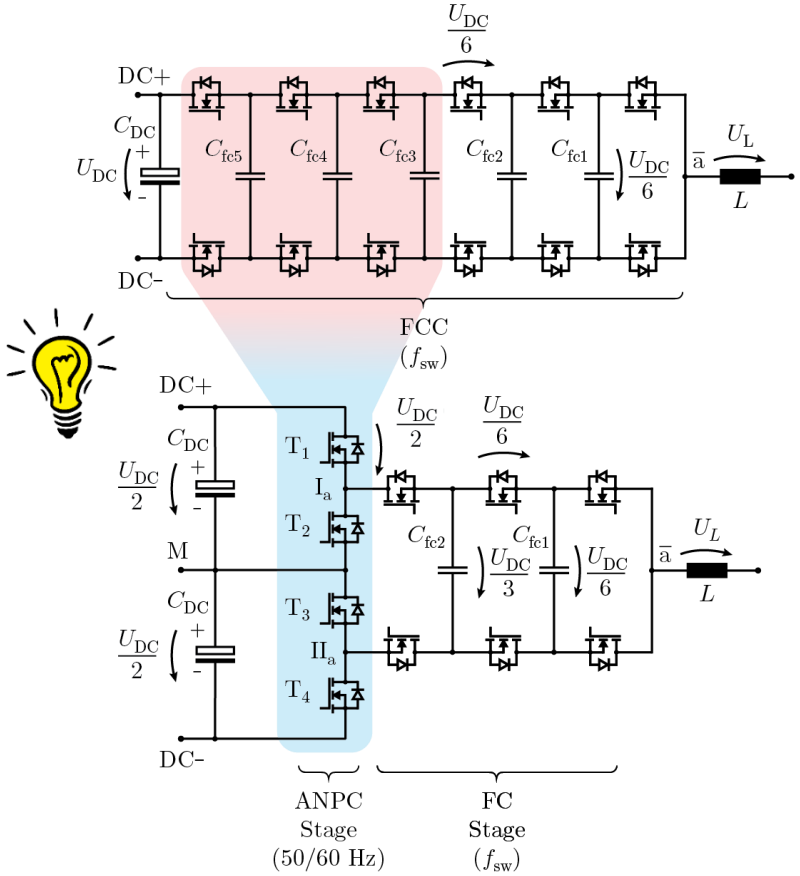


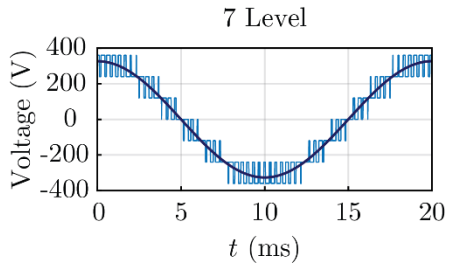


- *Hall Sensor Bandwidth f_{Hall} = 1.4 MHz*
- *Sense Wdg. Integrator Corner Frequency f_{int}=350 Hz*
- *Low/High-Pass Filter Cross-Over Network f_{filter} = 15 kHz*

3-Φ Hybrid Multi-Level Inverter

- *Realization of a 99%++ Efficient 10kW 3-Φ 400V$_{rms,ll}$ Inverter System*
- *7-Level Hybrid Active NPC Topology / LV Si-Technology*





99.35%
2.6kW/kg
56 W/in^3

- *200V Si → 200V GaN Technology Results in 99.5% Efficiency*

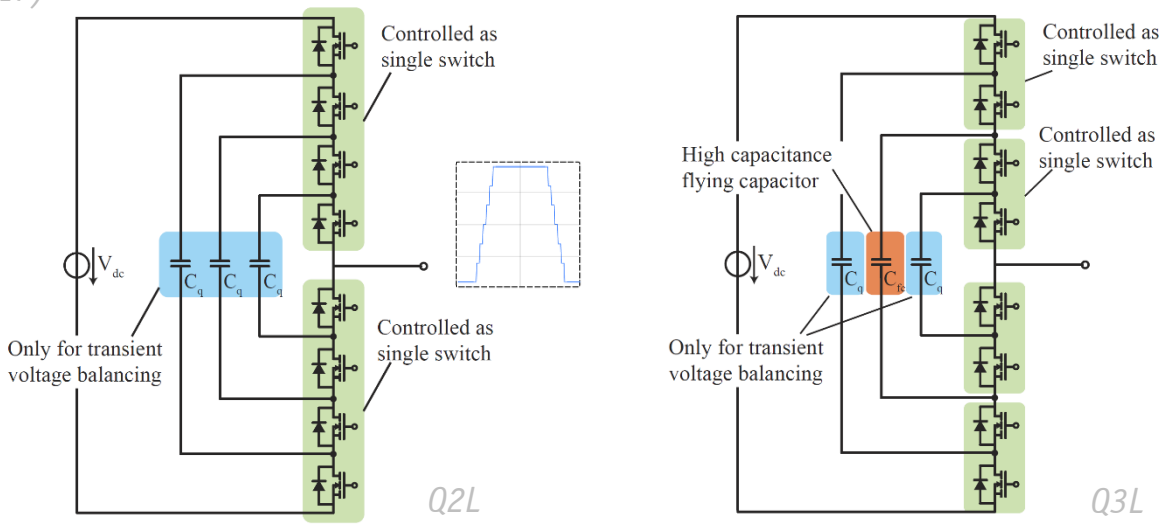
Quasi-2L/3L
Flying Capacitor Inverter

Quasi-2L & Quasi-3L Inverters

- *Operation of N-Level Topology in 2-Level or 3-Level Mode*
- *Intermediate Voltage Levels Only Used During Sw. Transients*
- *Applicability to All Types of Multi-Level Converters*

M. Schweizer (2017)

ABB

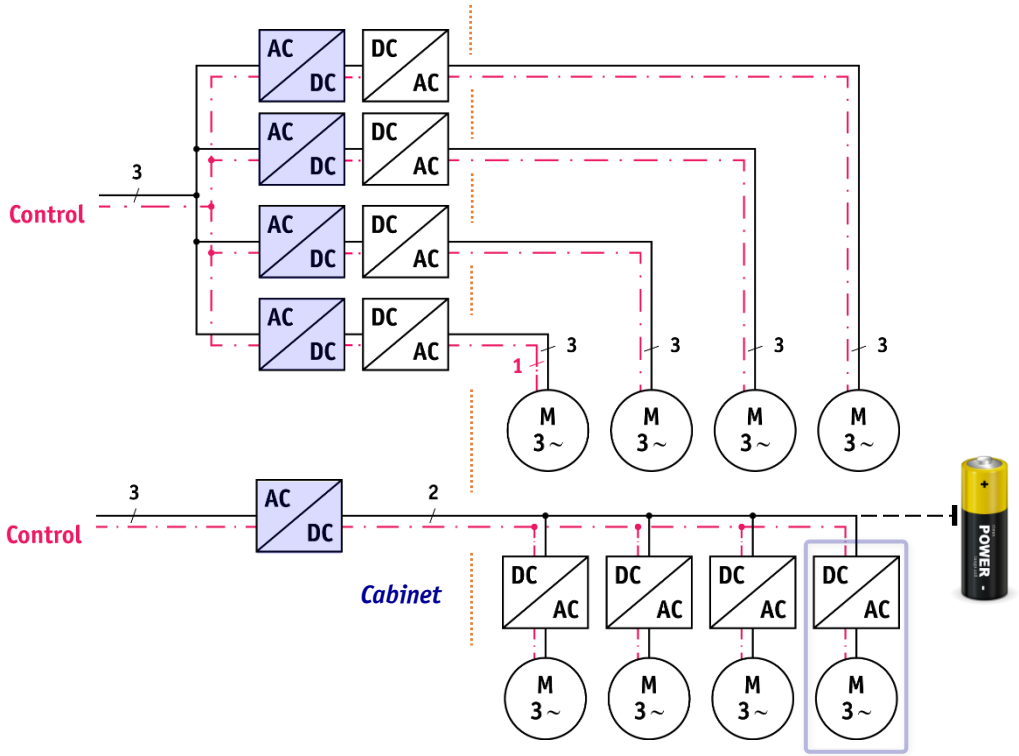


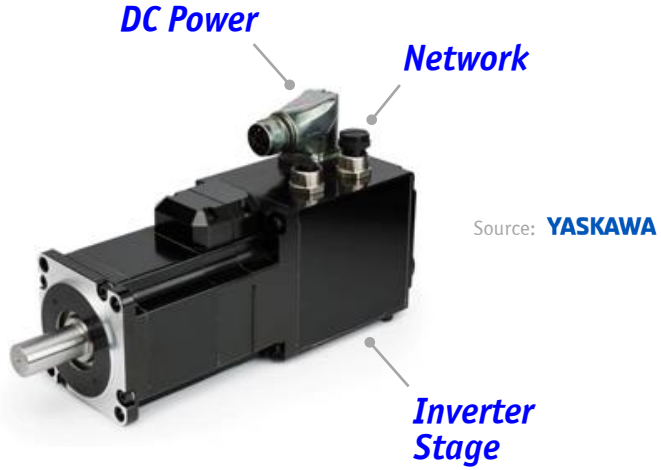
- *Reduced Avg. dv/dt → Lower EMI & Lower Overvoltages @ Motor Terminals*
- *Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors*
- *Low Voltage/Low $R_{DS(on)}$/Low $ MOSFETs → High Efficiency / No Heatsinks / SMD Packages*

Motor-Integrated Inverter Systems

Multi-Axis Drive Systems

- *Common DC-Bus — Single AC/DC Converter / Smaller Cabinet*
- *Motor Integration of DC/AC Stage — Massive Saving in Cabling Effort / Simplified Installation*



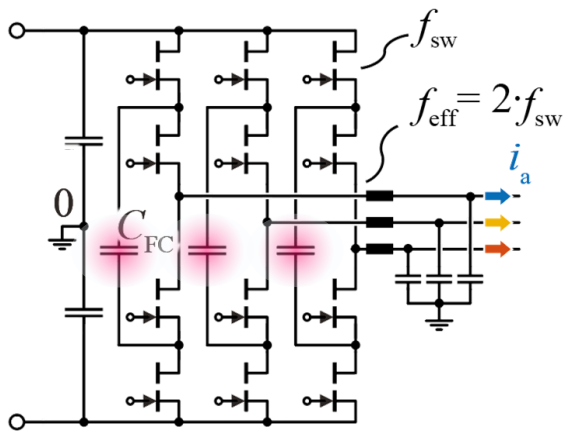


Source: YASKAWA

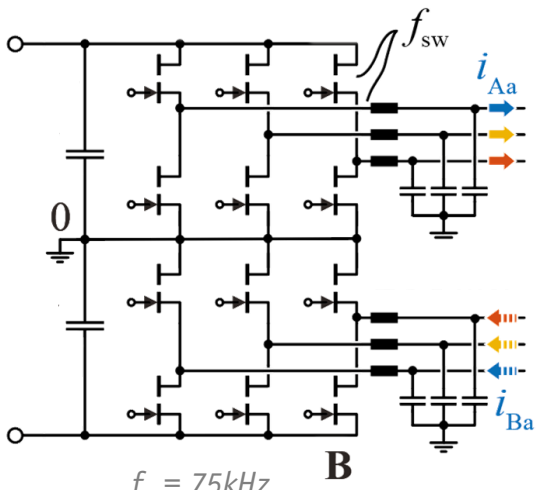
- *Facilitates DC-Bus Energy Buffer*
- *Direct Energy Exchange @ DC-Bus / Higher Efficiency / Unidirectional Front-End*

Motor-Integrated Inverter Stage

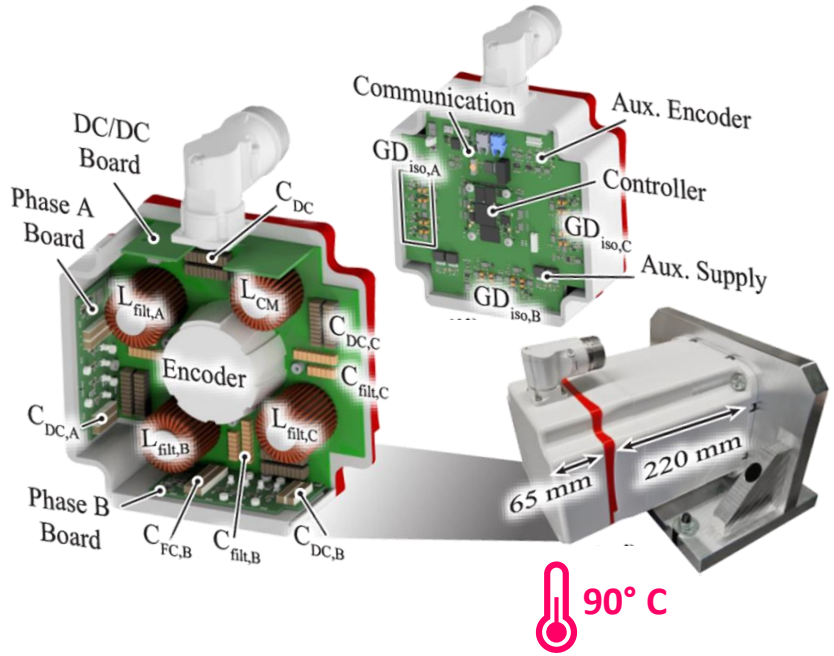
- *Comparative Evaluation of ML-Inverter Concepts*
- *2x 2-Level Stacked 650V GaN | 3-Level 650V GaN | 7-Level 200V Si Inverter*
- *Design for 800V DC-Link / 7.5kW / 99% Efficiency / 3s 3x T_N Overload*



f_{sw} = 35kHz



f_{sw} = 75kHz

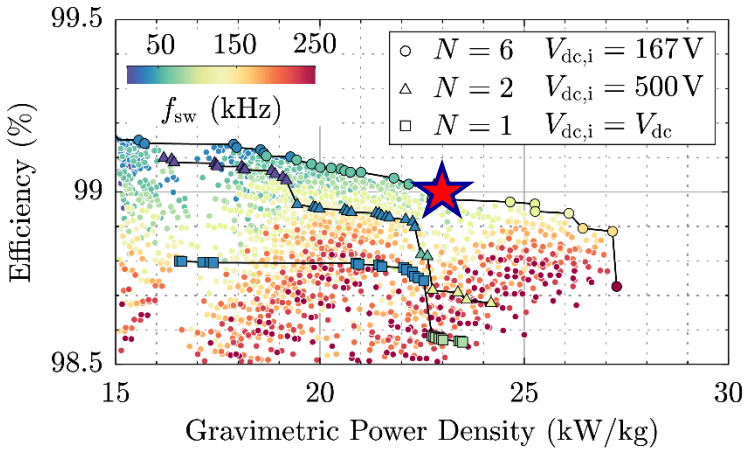


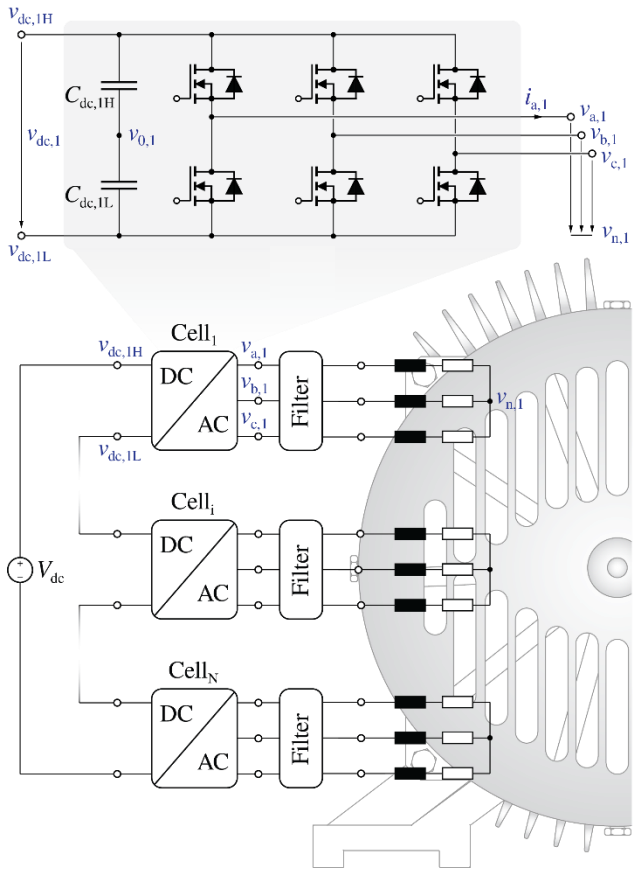
- *7-Level FC Inverter — Large PCB Area Requirement & High Complexity*
- *2x 2-Level Inverter — No Flying Capacitors & CM Cancellation / Low L_{CM} Volume*
- *3-Level FC Inverter — Best Overall Trade-Off (Complexity / PCB Area / Volume of Full-Sinewave Filter etc.)*

Stacked-Multi-Cell (SMC) Inverter

- *Fault-Tolerant VSD*
- *Low-Voltage Inverter Modules*
- *Very-High Efficiency / Power Density*
- *Automated Manufacturing*

- *Rated Power* *45 kW / f_{out} = 2 kHz*
- *DC-Link Voltage* *1 kV*

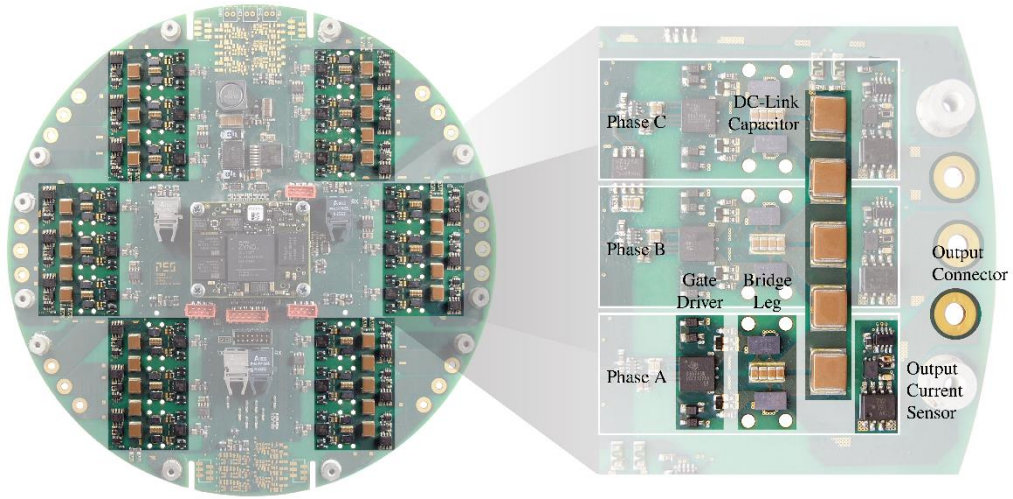




- *Smart Motor / All-in-One / Plug & Play* | *Connected / Intelligent VSD 4.0*

Motor-Integrated SMC-Inverter

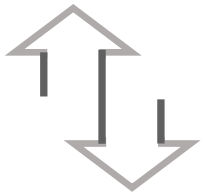
- *Rated Power* *9 kW @ 3700 rpm*
- *DC-Link Voltage* *650...720 V*
- *3-Φ Power Cells* *5+1*
- *Outer Diameter* *220 mm*



— *Axial Stator Mount*
— *200 V GaN e-FETs*
— *Low-Capacitance DC-Links*
— *45 mm x 58 mm / Cell*

- *Main Challenge — Thermal Coupling OR Thermal Decoupling of Motor & Inverter*

Buck-Boost Functionality

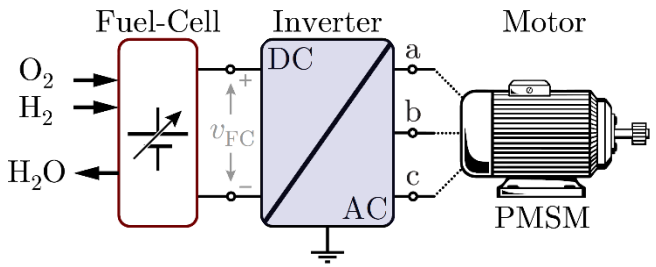


Motivation

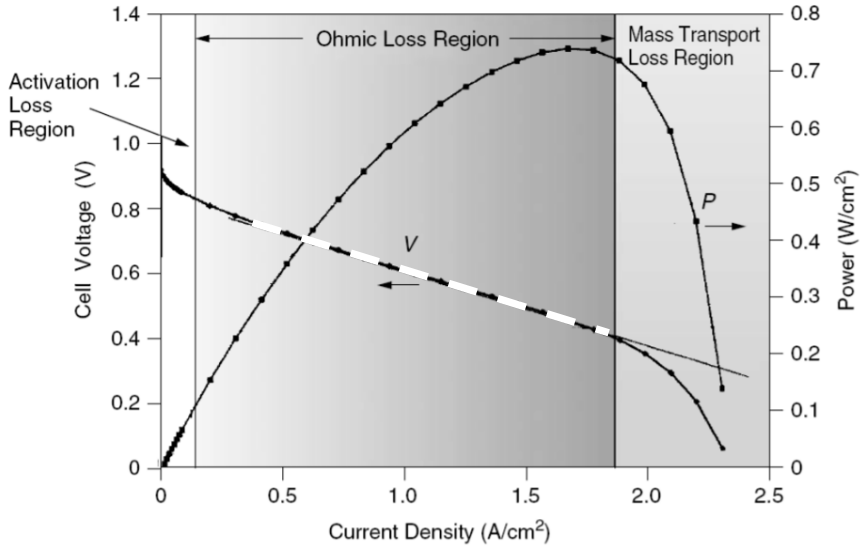
- *General / Wide Applicability*

— *Adaption to Load-Dependent Battery | Fuel Cell Supply Voltage*
— *Operation in Wide Output Voltage / Wide Motor Speed Range*

Source: magazine.fev.com



Source: www.chegg.com

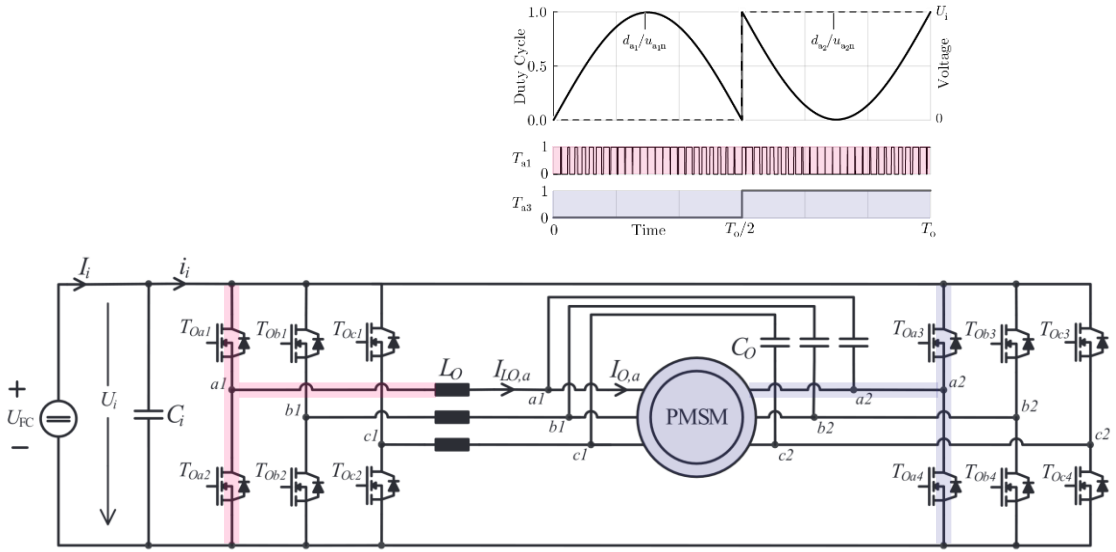


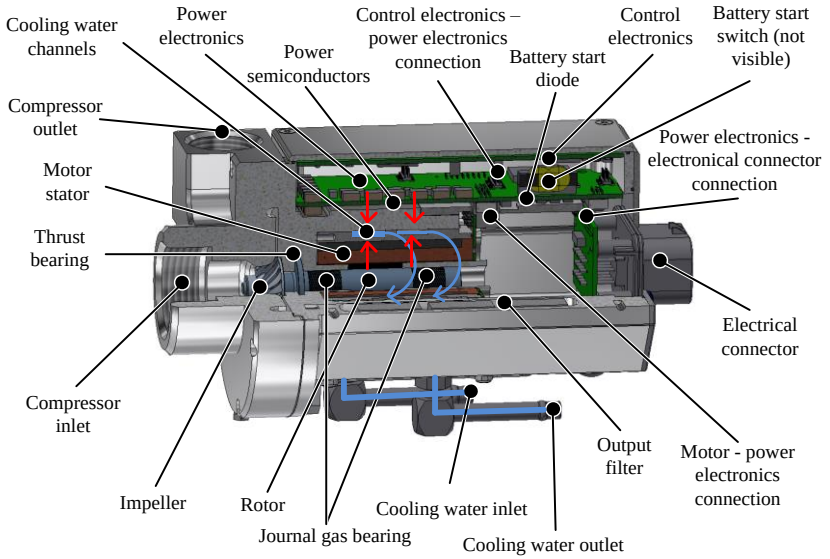
- *Full-Sinewave Filtered Motor Supply Voltage*
- *LC Output Filter Inductor Advantageously Utilized as Buck-Boost-Inductor*

Double-Bridge (DB) Inverter

Compressor-Integrated DB-GaN-Inverter

- *E-Mobility 5...15kW Fuel Cell Pressurized Air Supply*
- *1kW Rated Power | U_{FC} = 40...130V | f_{sw}=300kHz | n = 280'000rpm / f_{out}= 4.6kHz*
- *Low EMI / Low Cabling Effort*

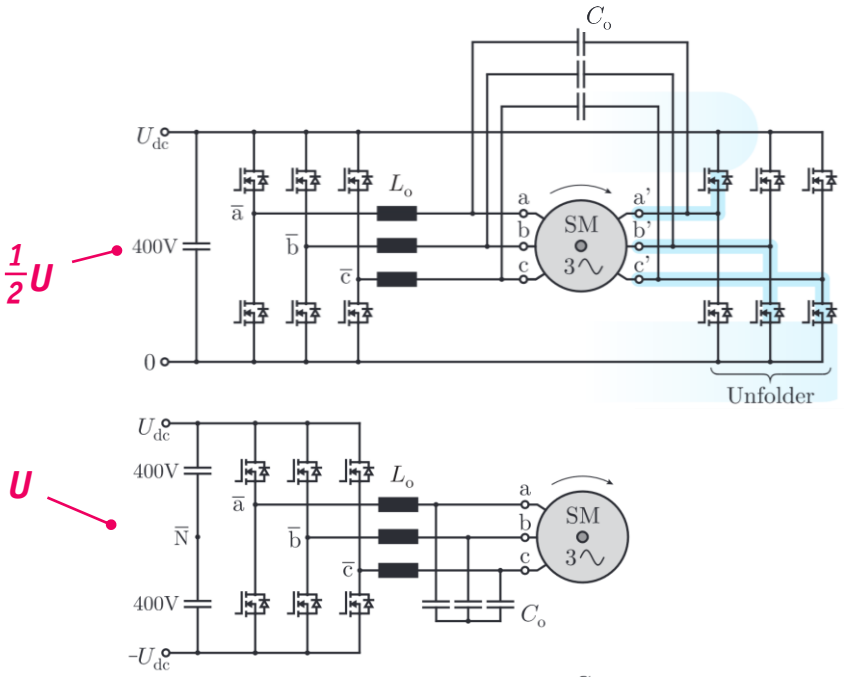


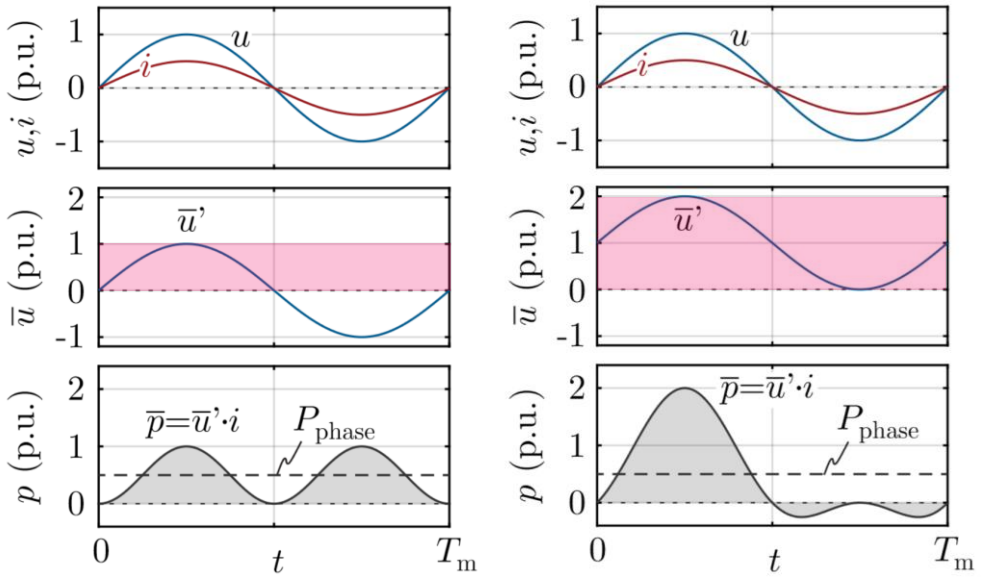


- *Integration → 2x System Power Density | 97% → 98.5% Inverter Efficiency*

Double-Bridge (DB)-Inverter Advantages

- *Unfolder → Factor 2 Lower DC-Link Voltage*
- *Lower Transistor Voltage Stress / Lower Switching Losses*
- *Conventional Inverter Bridge-Leg Processes 2x Instantaneous Peak Power*

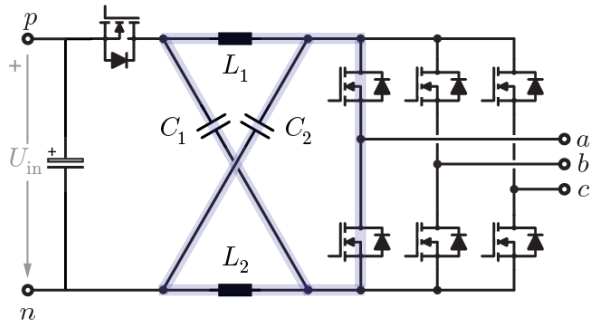




- *Access to All Wdg. Terminals — No Problem for Inverter/Motor Integration*

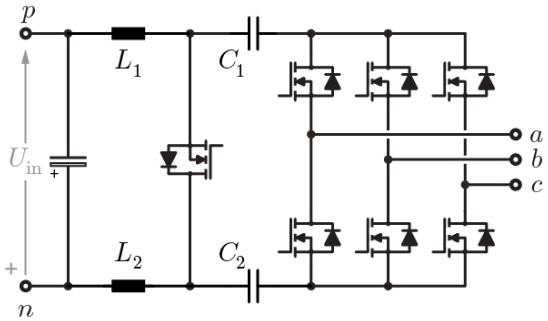
"Outside-the-Box" Topologies

- *Z-Source Inverter → Shoot-Through States Utilized for Boost Function*
- *Higher Component Stress Effectively Limits Boost Operation to ≈120% U_{in}*



Source: F.Z. Peng / 2003
J. Rabkowski / 2007

- *3-Φ Back-End DC/AC Cuk-Converter*

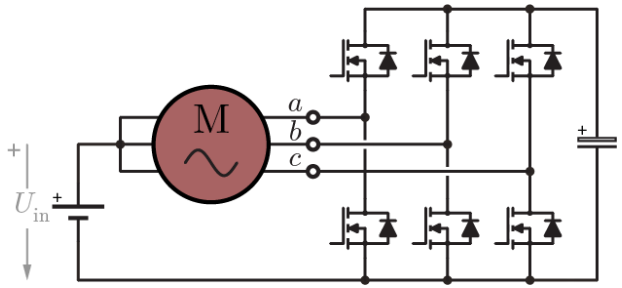


Source: T.A. Lipo
et al. /2002 &
K.D.T Ngo / 1984

- *Integration Typically Results in Higher Comp. Stresses & Cntrl. Complexity / Lower Performance*

Boost Converter DC-Link Voltage Adaption

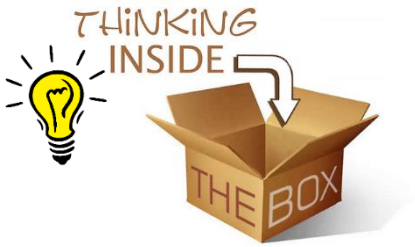
- *Inverter-Integr. DC/DC Boost Conv. → Higher DC-Link Voltage / Lower Motor Current*
- *Access to Motor Star-Point & Specific Motor Design Required*
- *No Add. Components*

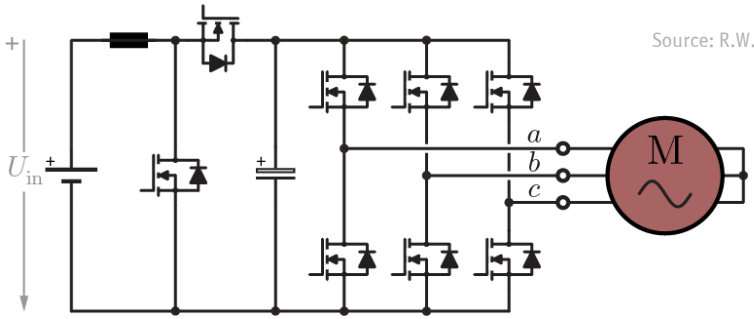


Source: J. Pforr et al. / 2009

- *Explicit Front-End DC/DC Boost-Stage*

Source: www.rick-gerber.com



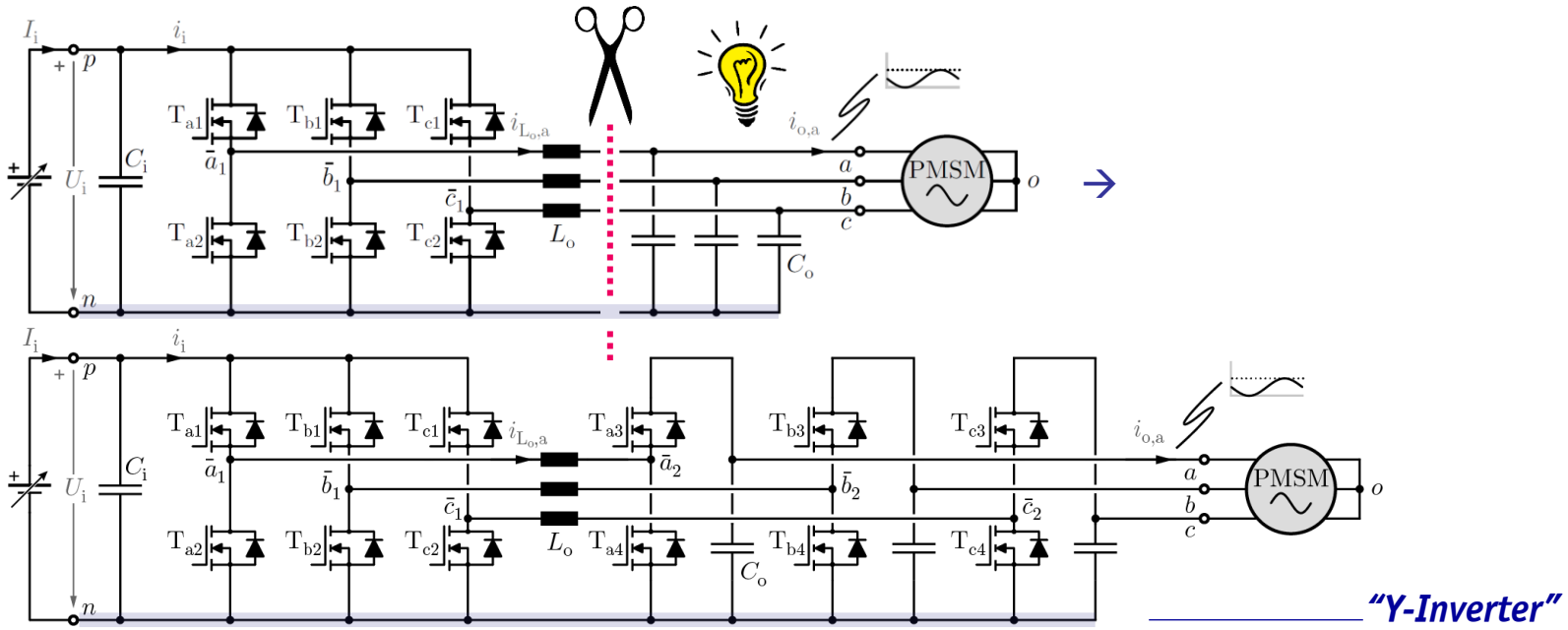


Source: R.W. Erickson et al. / 1986

- *Coupling of the Control of Both Converter Stages → "Synergetic Control"*

Buck-Boost «Y-Inverter»

- *Generation of AC-Voltages Using Unipolar Bridge-Legs*

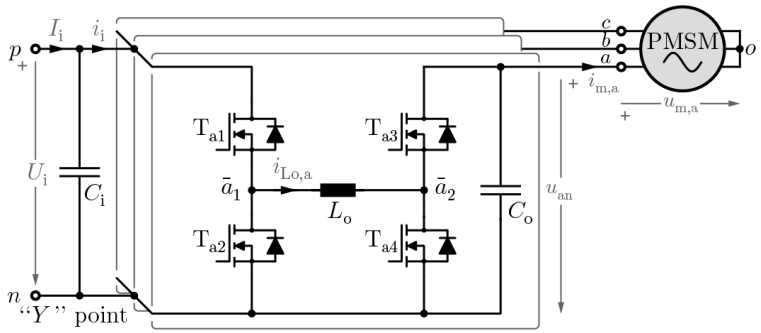


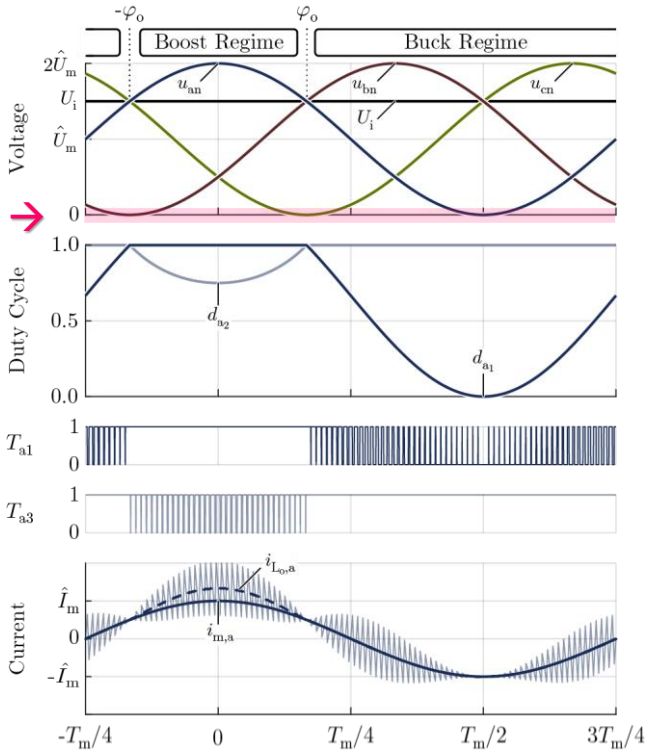
"Y-Inverter"

- *Switch-Mode Operation of Buck OR Boost Stage → Quasi Single-Stage Energy Conversion (!)*
- **3-Φ Continuous Sinusoidal Output / Low EMI** *→ No Shielded Cables / No Motor Insul. Stress*

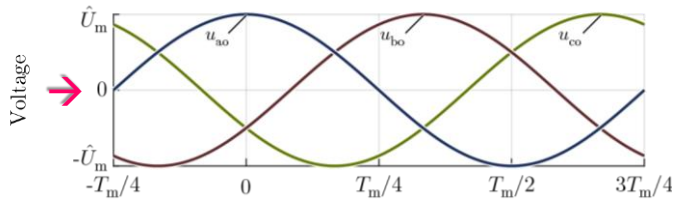
Sinusoidal Modulation

- ***Y-Inverter***





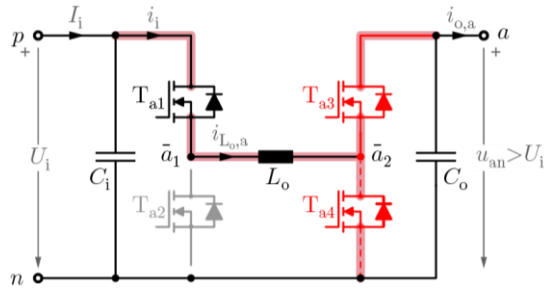
- ***Motor Phase Voltages***



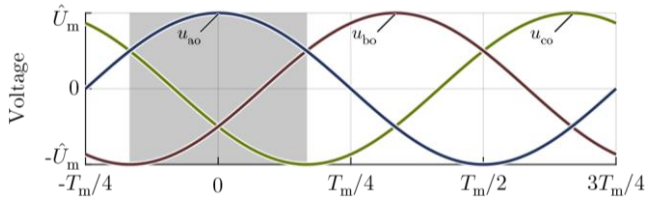
- ***Const. DC Offset → Strictly Positive Output Voltages u_{aN}, u_{bN}, u_{cN}***
- ***Mutually Exclusive Operation of the Half-Bridges → Low Switching Losses***

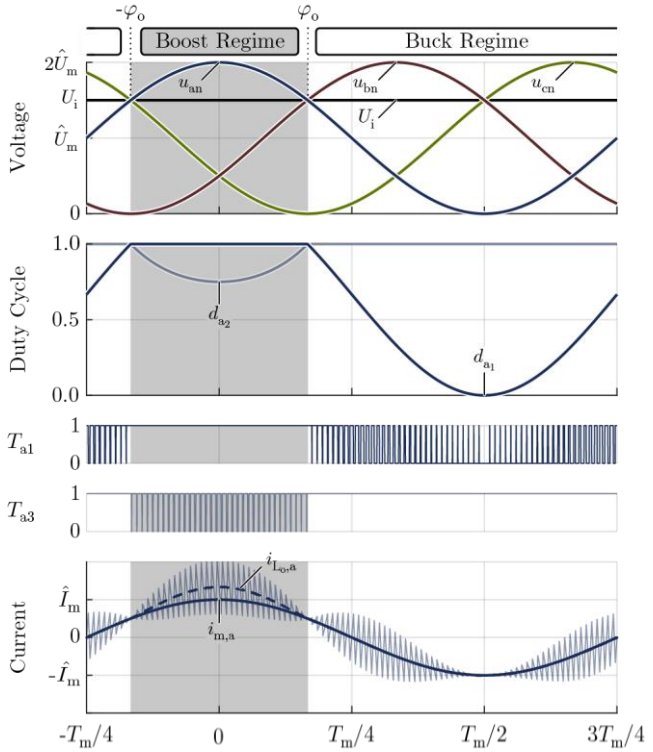
Boost-Operation $u_{an} > U_i$

- *Phase-Module*



- *Motor Phase Voltages*

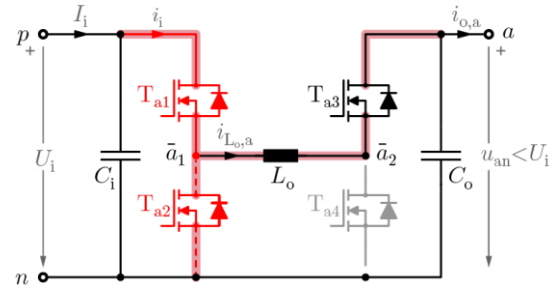




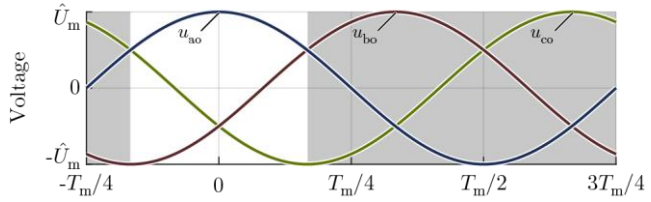
- *Current-Source-Type Operation*
- *Clamping of Buck-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion*

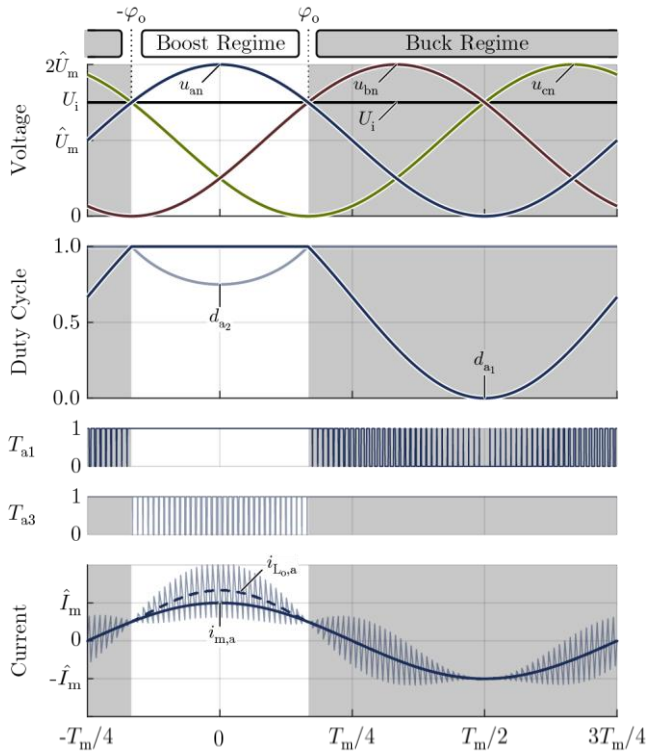
Buck-Operation $u_{an} < U_i$

- ***Phase-Module***



- ***Motor Phase Voltages***

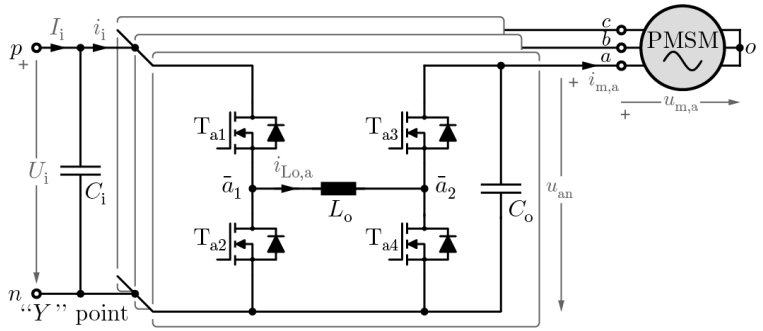


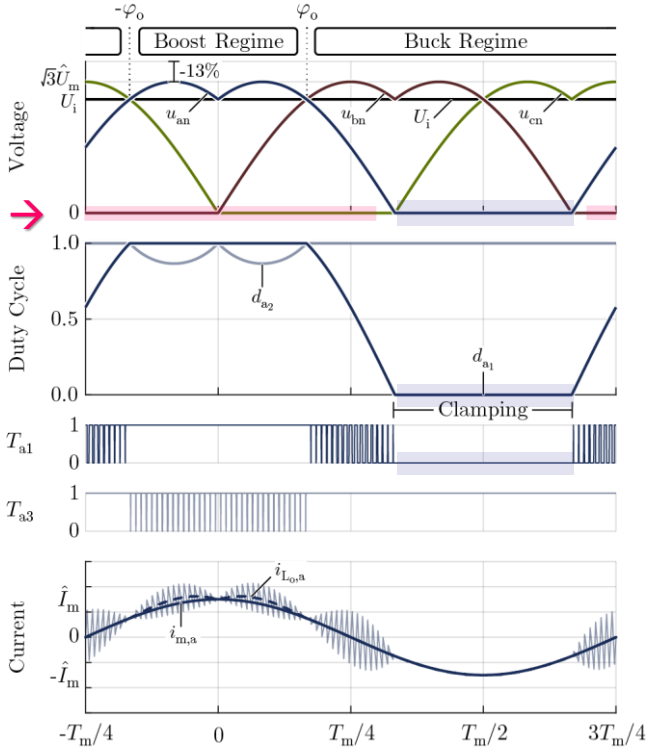


- ***Voltage-Source-Type Operation***
- ***Clamping of Boost-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion***

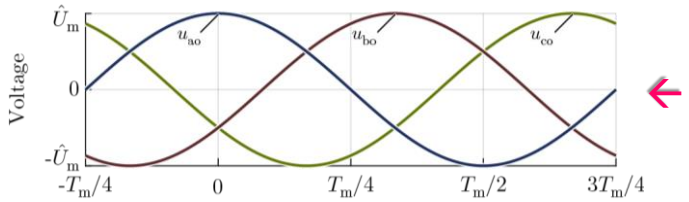
Discontinuous Modulation

- ***Y-Inverter***





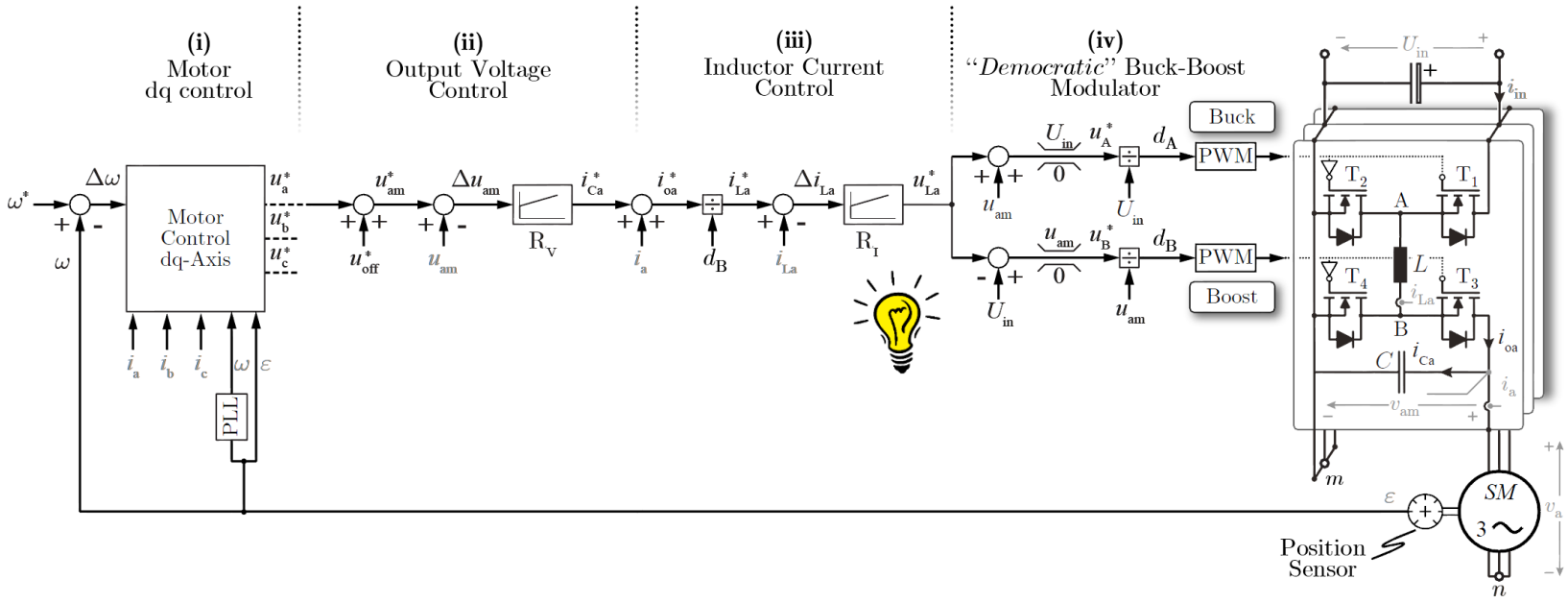
- ***Motor Phase Voltages***



- ***Clamping of Each Phase for 1/3 of the Fund. Period → Low Switching Losses (!)***
- ***Non-Sinusoidal Module Output Voltages BUT Sinusoidal Line-to-Line Voltages***

Control Structure

- *Motor Speed Control*

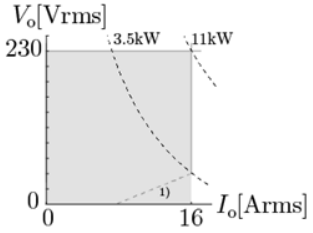


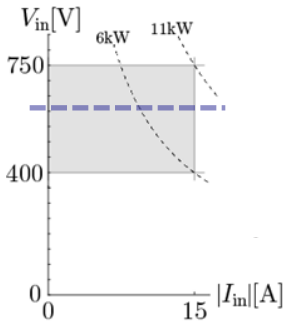
- *Cascaded Motor Current / Output Voltage / Inductor Current Control Loops*
- *Seamless Transition between Boost- & Buck-Mode → "Democratic" Control*

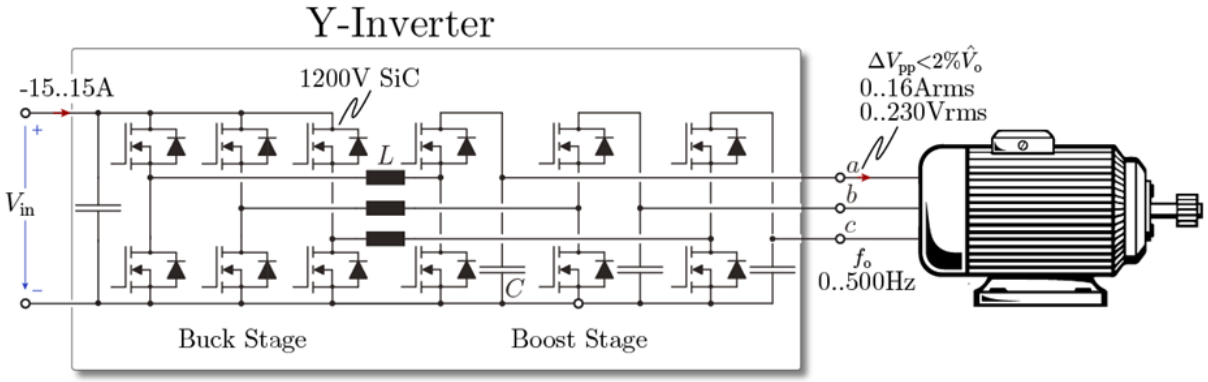
Y–Inverter VSD

- *Demonstrator Specifications*

- Wide DC Input Voltage Range → 400...750V_{DC}
- Max. Input Current → ± 15A



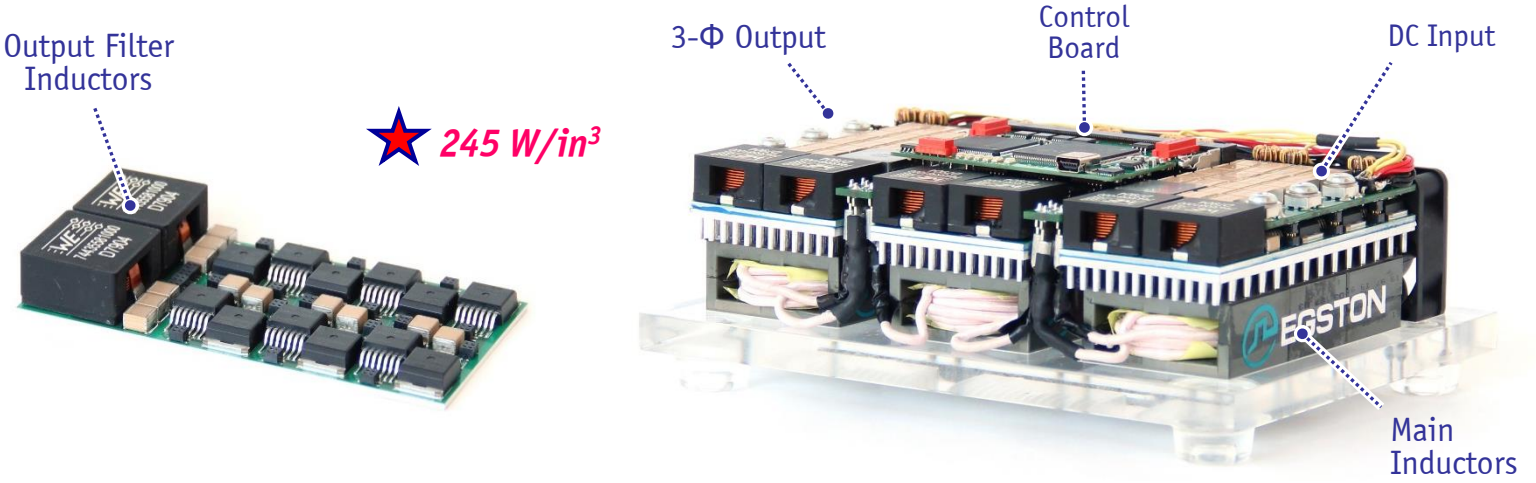




- Max. Output Power → 6...11 kW
- Output Frequency Range → 0...500Hz
- Output Voltage Ripple → 3.2V Peak @ Output of Add. LC-Filter

Y-Inverter Demonstrator

- DC Voltage Range 400...750V_{DC}
- Max. Input Current ± 15A
- Output Voltage 0...230V_{rms} (Phase)
- Output Frequency 0...500Hz
- Sw. Frequency 100kHz
- 3x SiC (75mΩ)/1200V per Switch
- IMS Carrying Buck/Boost-Stage Transistors & Comm. Caps & 2nd Filter Ind.



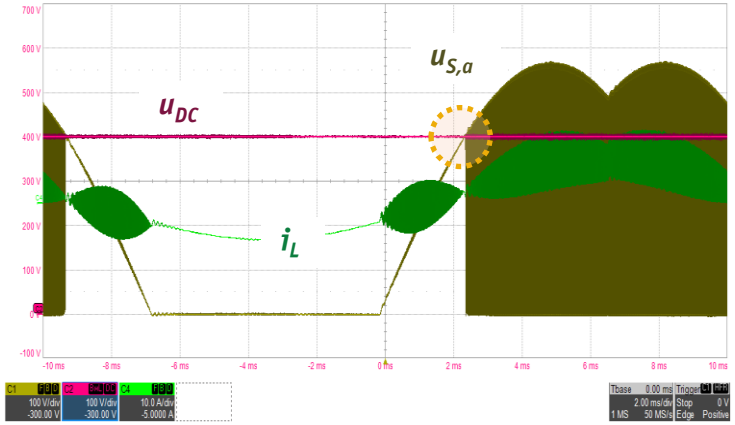
- Dimensions → 160 x 110 x 42 mm^3

Y–Inverter - Measurement Results

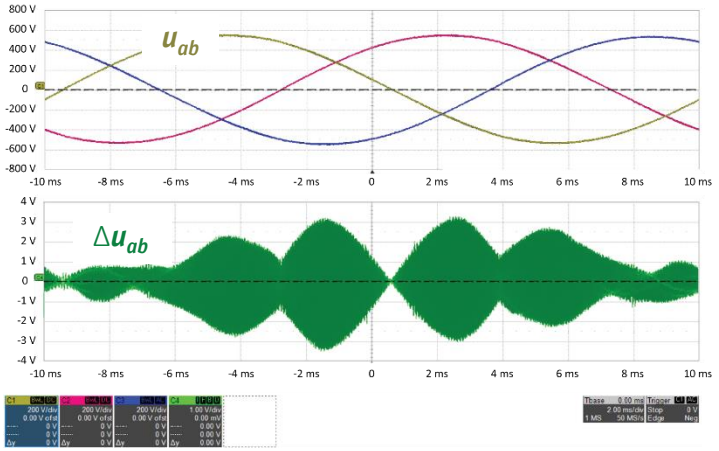
- *Stationary Operation*

U_{DC}= 400V
U_{AC}= 400V_{rms} (Motor Line-to-Line Voltage)
f_O = 50Hz
f_{sw} = 100kHz / *Discontinuous PWM*
P = 6.5kW

100V/div
10A/div



200V/div
1V/div

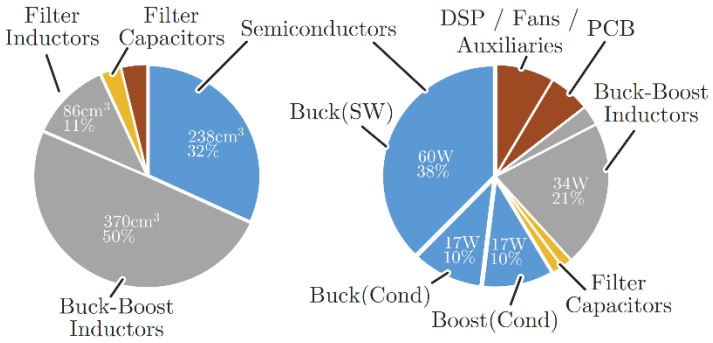


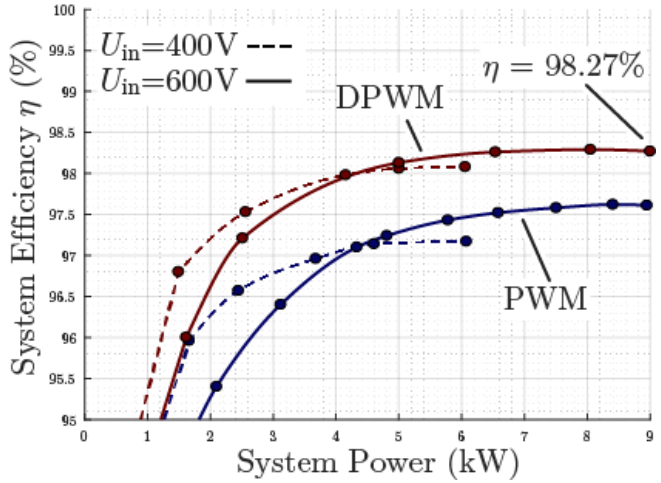
- *Line-to-Line Output Voltage Ripple < 3.2V*

Efficiency Measurements

- *Dependence on Input Voltage & Output Power Level*

U_{DC}= 400V / 600V
U_{AC}= 230V_{rms} (Motor Phase-Voltage)
f_{sw} = 100kHz

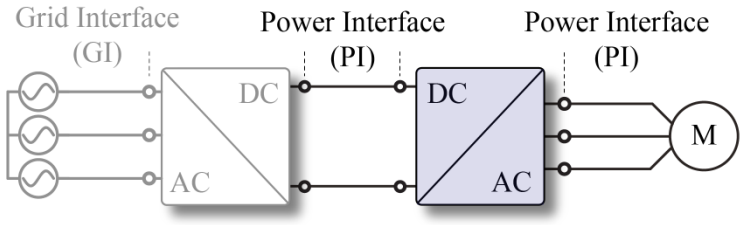


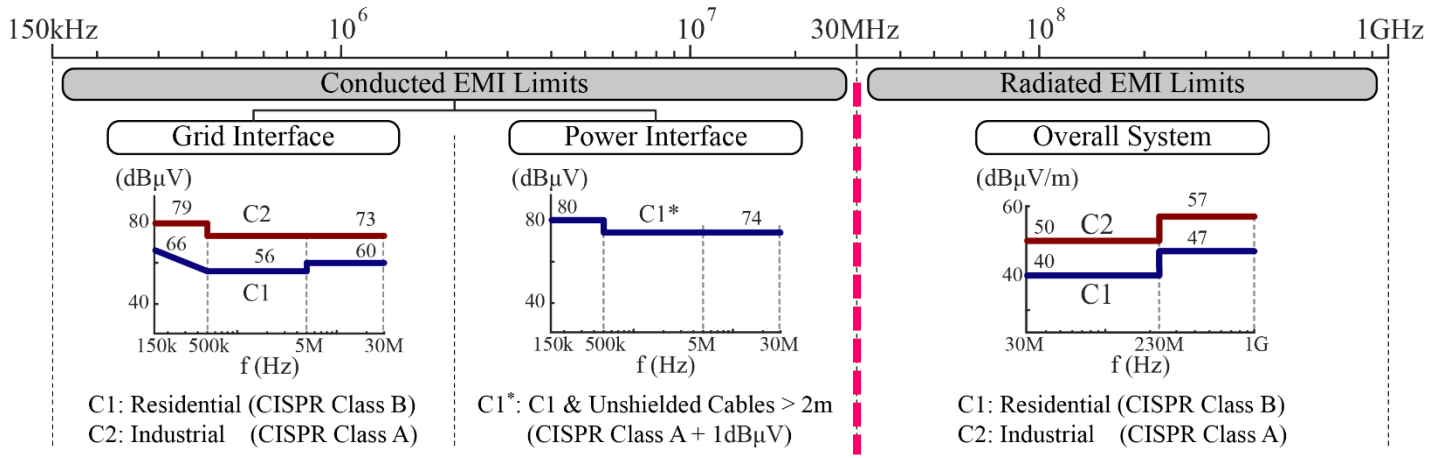


- *Multi-Level Bridge-Leg Structure for Increase of Power Density @ Same Efficiency*

EMI-Limits (VSD Product Standard)

- *IEC 61800-3* → *Product Standard for Variable-Speed Motor Drives*
- *EMI Emission Limits* → *Grid Interface (GI) and Power Interfaces (PI)*
- *Application* → *Residential (C1) or Industrial (C2)*

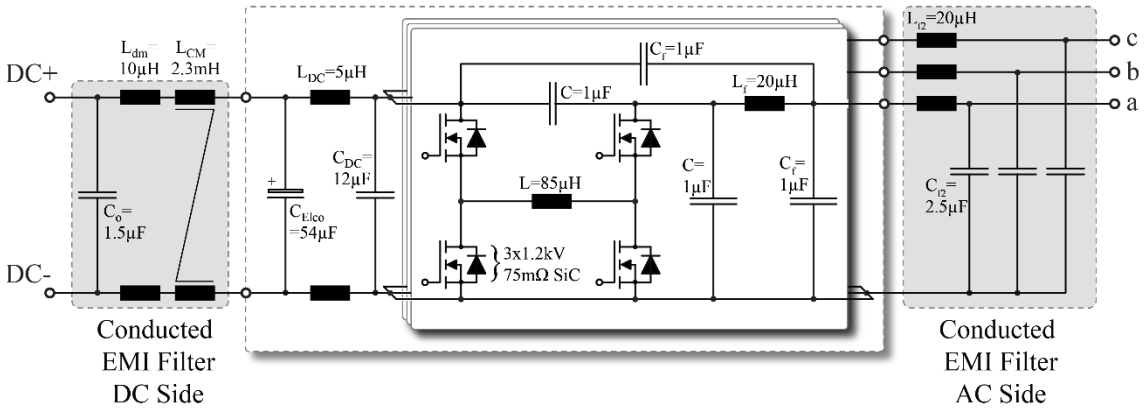


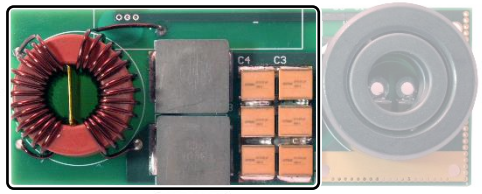


- *EMI-Filter Design for Unshielded Cables > 2m and Resid. Applications (Cond. & Rad.)*

Conducted EMI-Filter

- *Separate Cond. DM & CM EMI-Filter on DC-Side & DC-Minus Ref. EMI-Filter on AC-Side*





L_{CM} L_{DM} $C_{DM} = C_0$

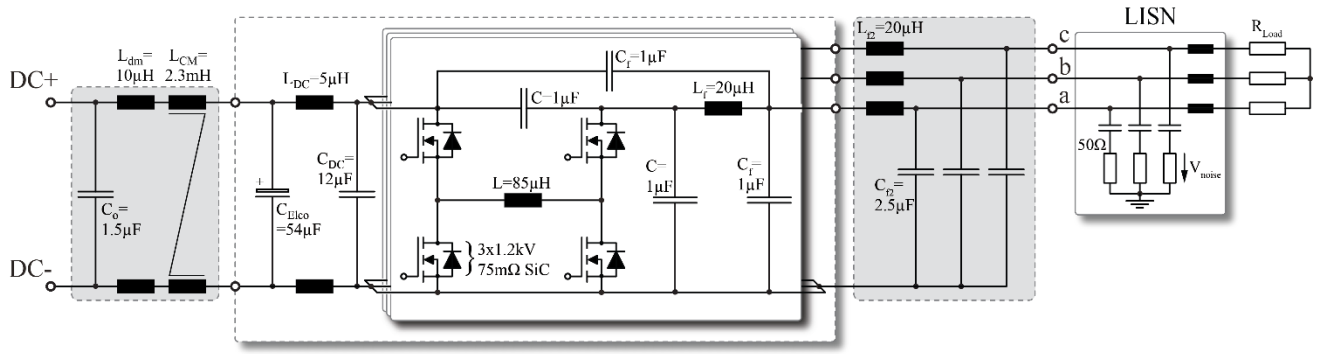
C_{f2} (on the back)

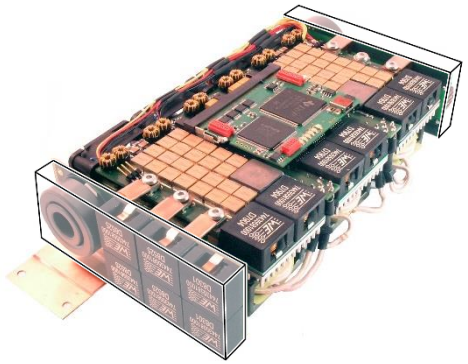
L_{f2}

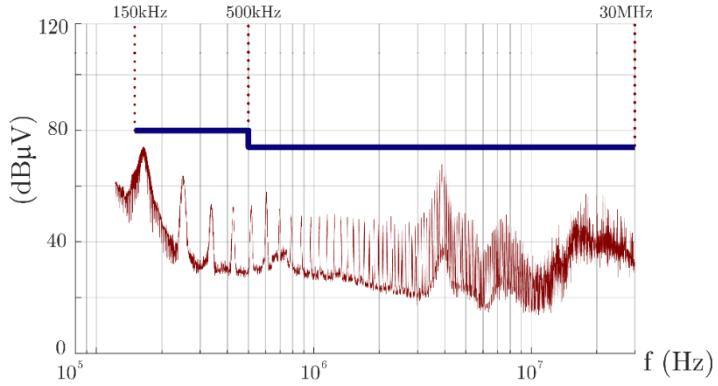
- *Low Add. EMI Filter Volume — 74cm³ for Each Filter (incl. Toroid. Radiated EMI Filter)*
- *Total Power Density Reduces — 15kW/dm³ (740cm³) → 12kW/dm³ (890cm³)*

Conducted EMI - Experimental Results

- *Measurements of the Cond. EMI Noise on the AC-Side (QP, with 50Hz AC-LISN)*



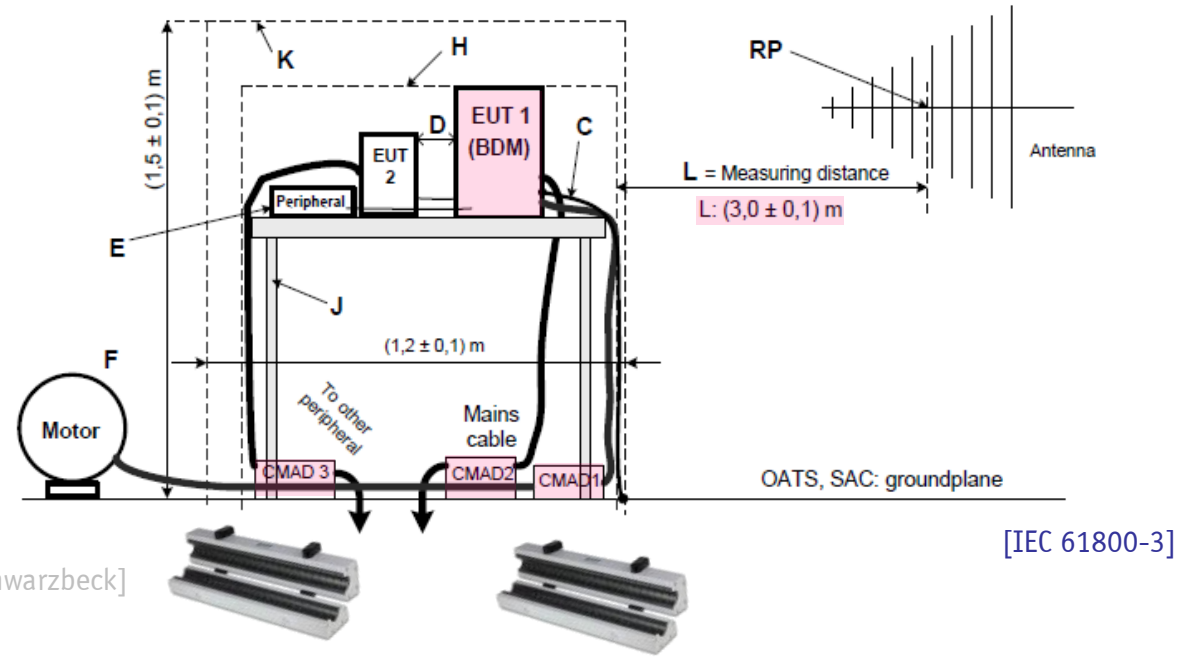




- *Small 80uH CM-Ind. Added on AC-Side - (3 cm³ of Add. Volume = 0.5% of Converter Vol.)*
- *Conducted EMI with Unshielded Motor Cable Fulfilled*

Measurement of Radiated EMI-Noise 1/2

- *Equipment Under Test (EUT) Placed on Wooden Table with Specified Arrangement*
- *CM Absorption Devices (CMAD) Terminate All Cables on AC-Side & DC-Side (Total $l_{cable} \approx 1.5m$)*
- *Measurement of Radiated Noise with Antenna in 3m Distance*



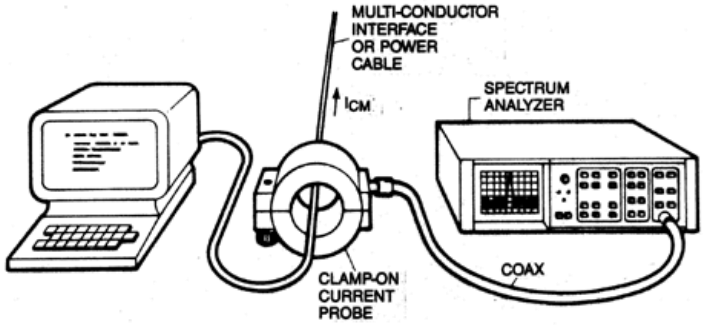
[Schwarzbeck]

[IEC 61800-3]

- *Either Open-Area Test Site (OATS) or Special Semi-Anechoic Chamber (SAC) Needed*
- *Alternative Pre-Compliance Measurement Method*

Measurement of Radiated EMI-Noise 2/2

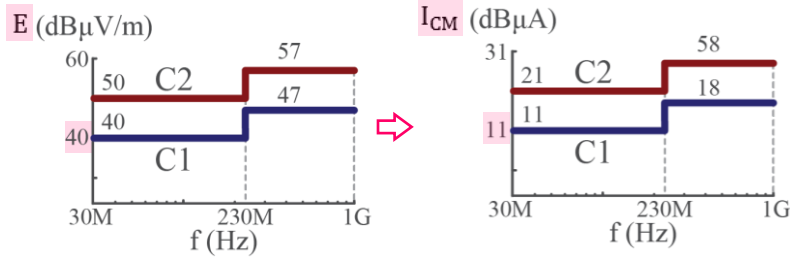
- *CM-Currents NOT Returning IN THE CABLE are the Dominant Source of Radiation*
- *Relation Between Radiated Electric Field and CM-Currents (!)*



$$E = \begin{cases} \dfrac{\mu_0 \cdot f \cdot l_{cable} \cdot I_{cm}}{r} & \dfrac{\lambda}{4} \leq l_{cable} \\ \dfrac{\mu_0 \cdot \frac{c_0}{4} \cdot I_{cm}}{r} & \dfrac{\lambda}{4} > l_{cable} \end{cases}$$

[Electromagnetic Compatibility Engineering, H. Ott]

[Fischer FCC F-33-1]
up to 250MHz
Z_{nom} = 6.3Ω

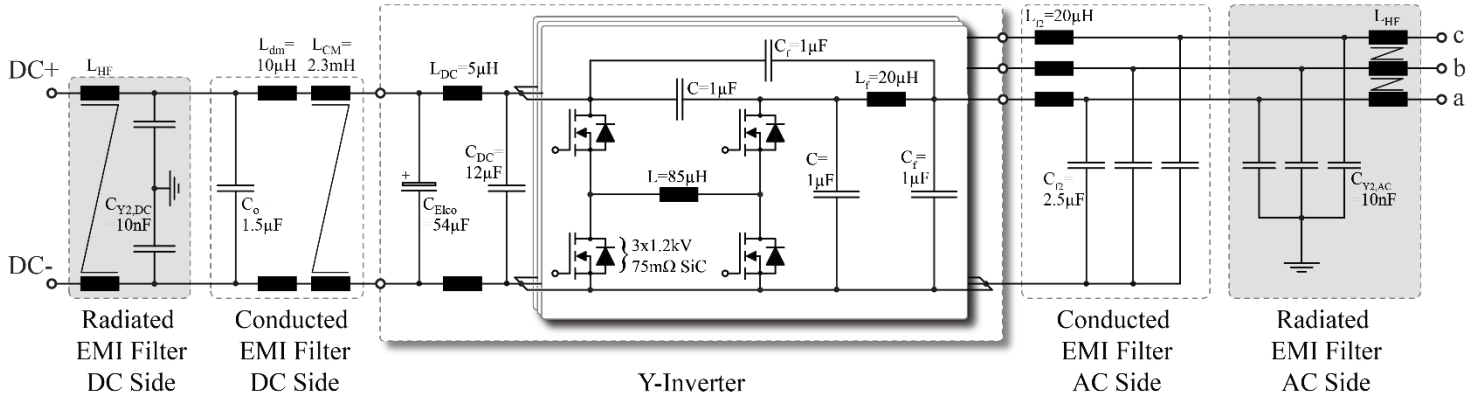


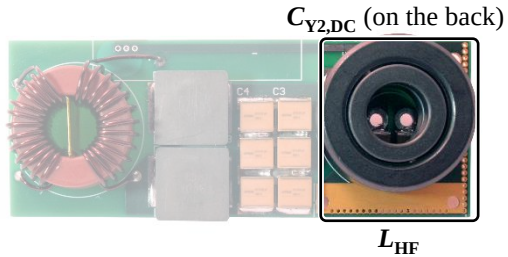
C1: Residential (CISPR Class B)
C2: Industrial (CISPR Class A)

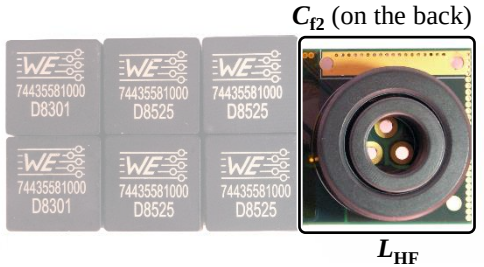
- *Max. Allow. El. Field Strength of 40dBuV/m → Max. CM-Current of 3.5uA (11dBuA)*
- *Current Probe Impedance of 6.3Ω (F-33-1) → Max. Noise Volt. of 26dBuV @ Test Receiver*

Radiated EMI-Filter Design

- *Single-Stage HF CM-Filter on DC-Side and AC-Side*
- *Plug-On CM-Cores (NiZn-Ferrites) → Low Parasitics & Good HF-Att. up to 1GHz*



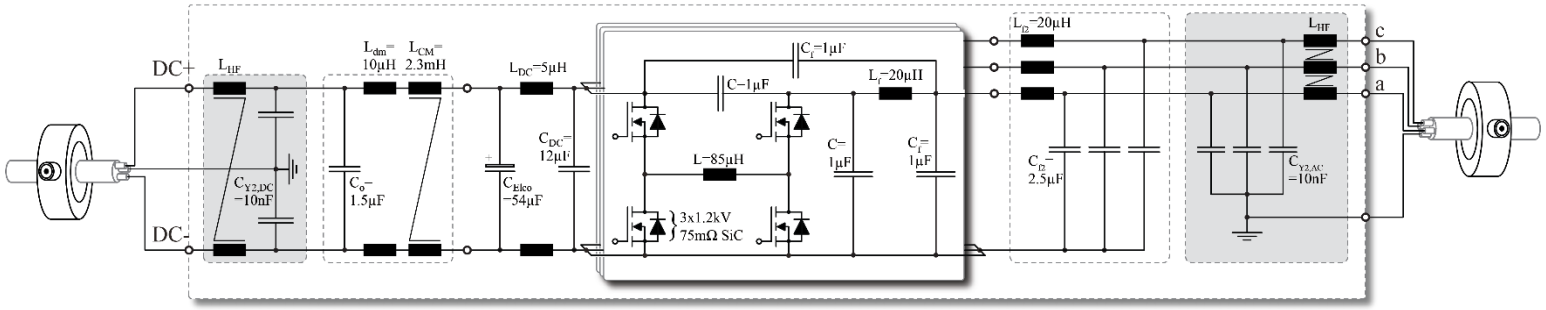


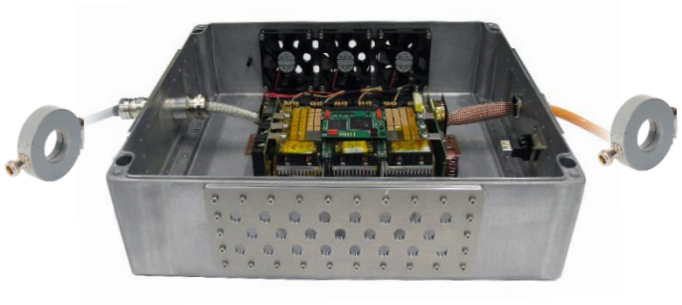


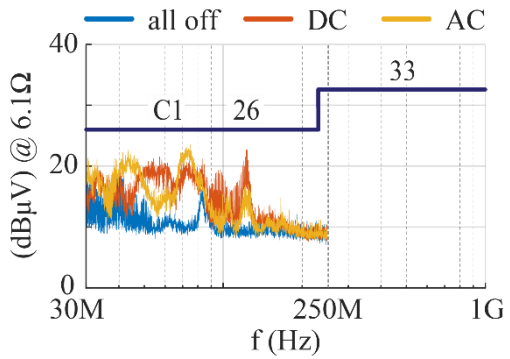
- *Additional EMI Filter Volume Already Considered with Conducted EMI Filter*
- *Total Power Density Slightly Reduces — 15 kW/dm³ → 12 kW/dm³*

Experimental Results - Radiated EMI

- *Y-Inverter Placed in Metallic Enclosure* → *Emulates Housing, but Motor Cables Un-Shielded (!)*
- *Measurement Setup* → *According IEC 61800-3*
- *Alternative Measurement Principle* → *Conducted CM-Current Instead of Radiation*



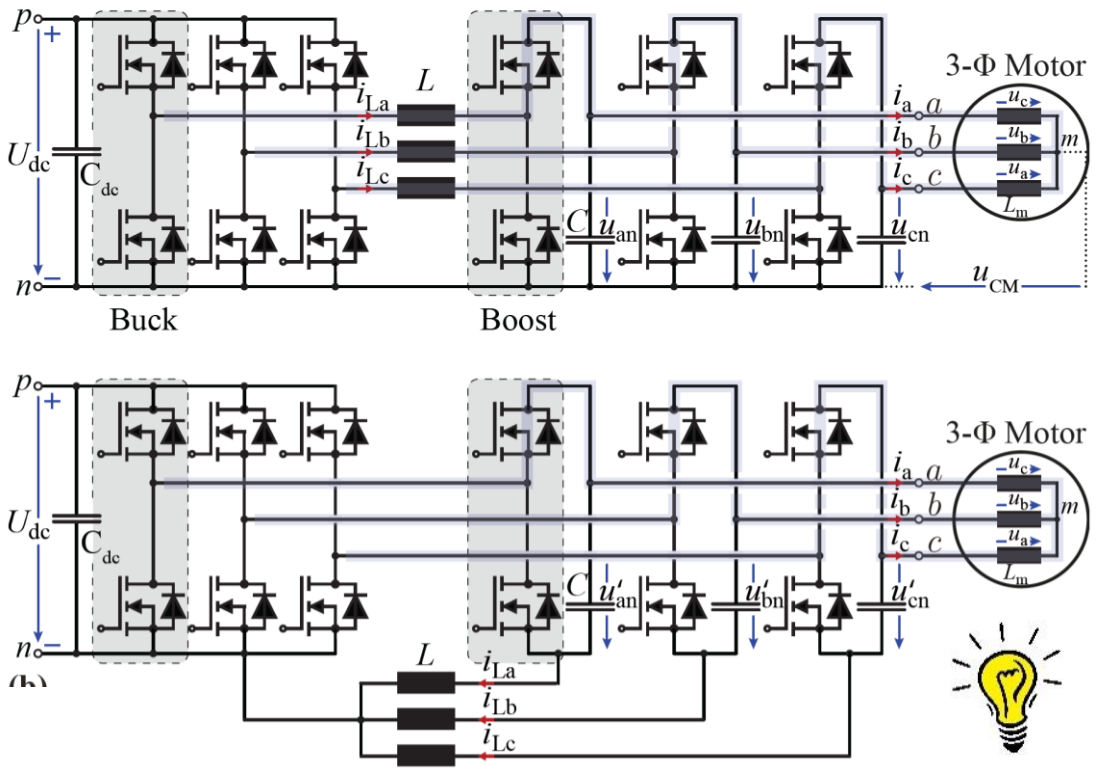




- *Already Noticeable Noise Floor*
- *HF-Emissions Well Below Equivalent EMI-Limit* → *Final Step: Verification Using Antenna*

Return-Path-Inductor Y-Inverter 1/2

- *Buck-Boost Y-Inverter Inductors* Relocated from Forward Current to Return Current Path
- *Up to 90% Reduction of Inductor Area Product | −80% of Magnetics Volume*



- *FPI-Y — Applicable for Ohmic OR Inductive Load / Sinusoidal Motor Phase Voltages*
- *RPI-Y — Applicability Limited to Inductive Load / PWM Motor Phase Voltages*

Return-Path-Inductor Y-Inverter 2/2

- *Buck-Boost Y-Inverter Inductors* Relocated from Forward Current to Return Current Path
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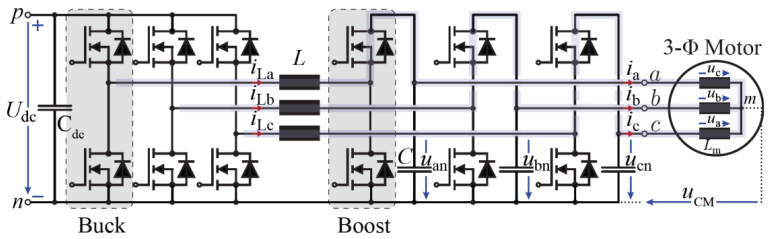
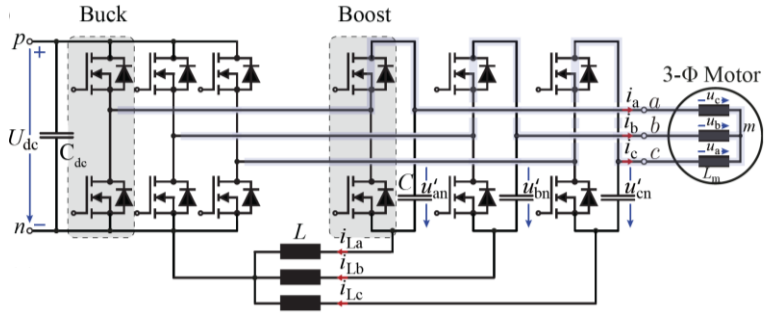
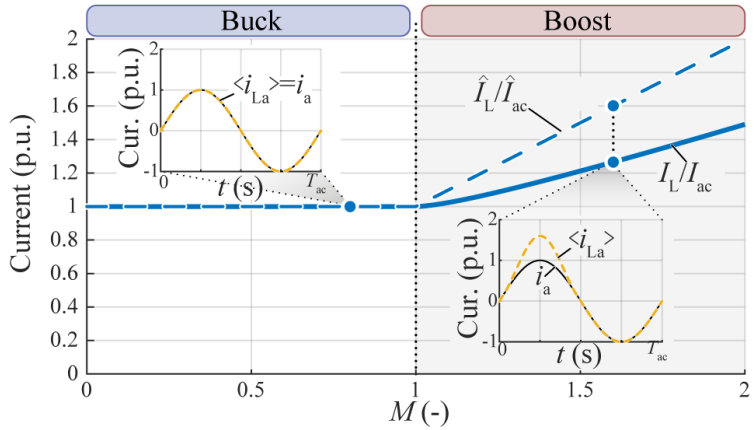
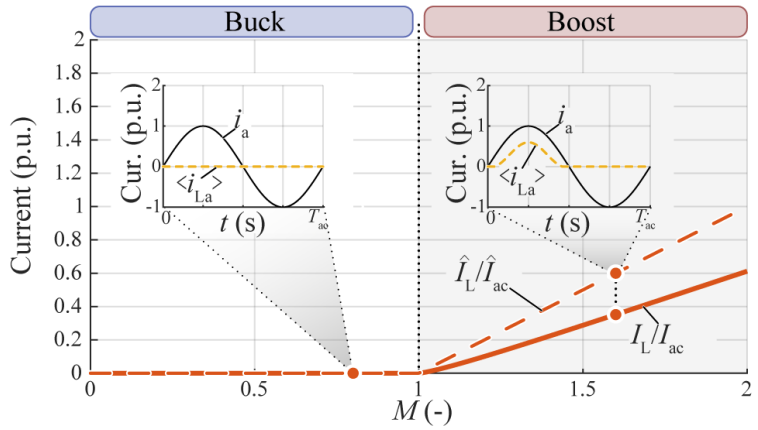






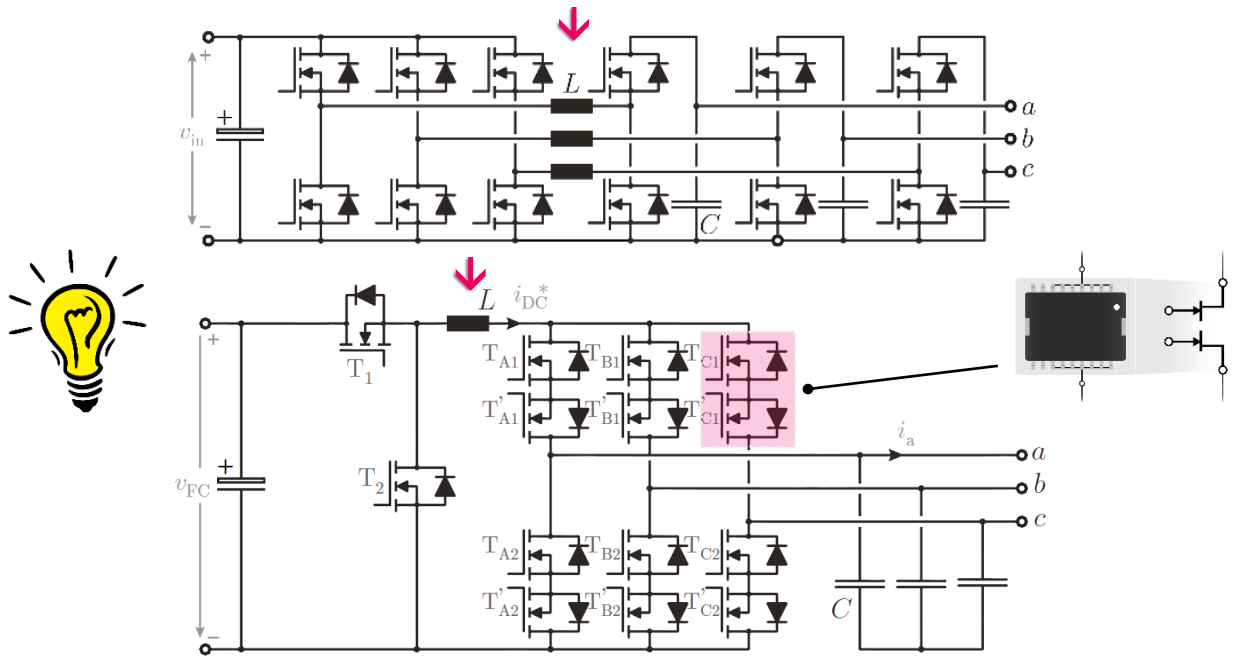


- *FPI-Y — Applicable for Ohmic or Inductive Load / Sinusoidal Motor Phase Voltages*
- *RPI-Y — Applicability Limited to Inductive Load / PWM Motor Phase Voltages*

3-Φ Current Source Inverter Topology

3-Φ Current Source Inverter (CSI) Topology

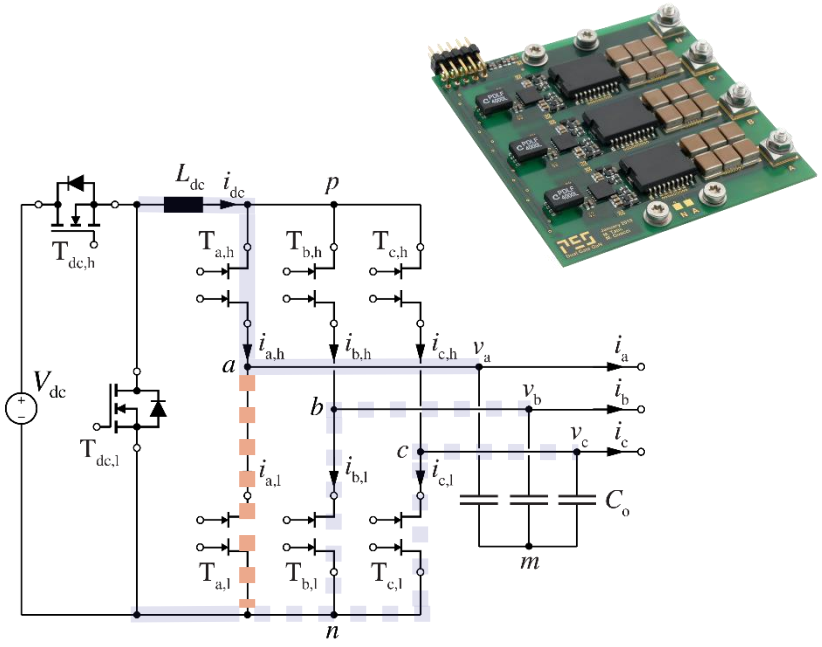
- *Y-Inverter → Phase Modules w/ Buck-Stage | Current Link | Boost-Stage*
- *3-Φ CSI → Buck-Stage V→I Converter | Current DC-Link DC/AC-Stage*

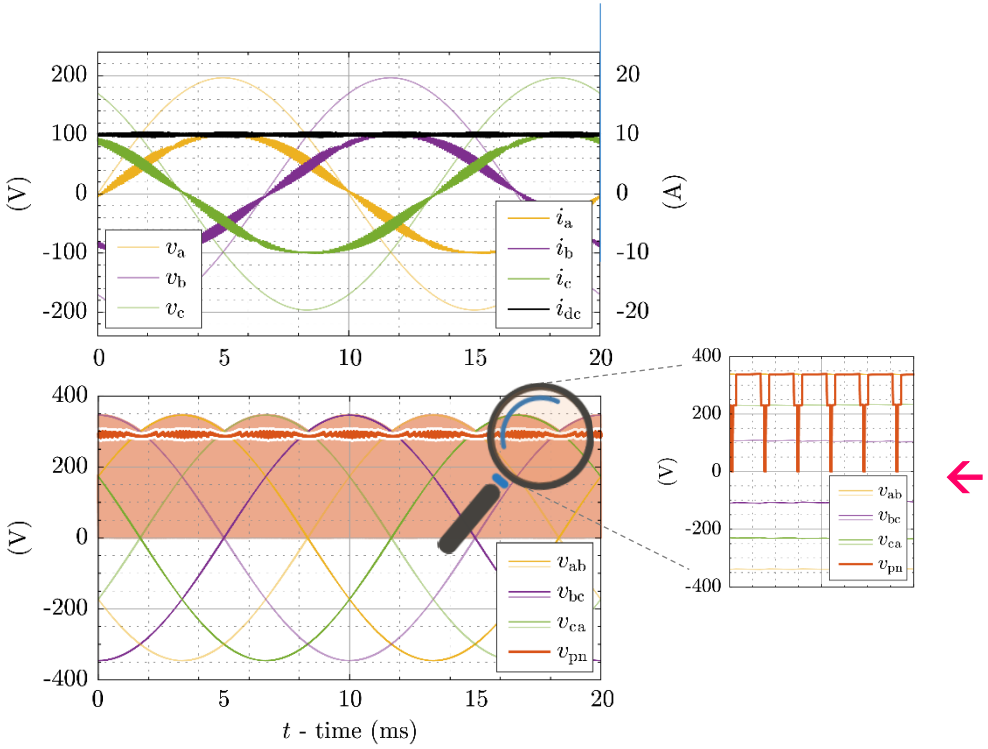


- *Single Inductive Component*
- *Positive DC-Side Voltage for Both Directions of Power Flow → Future Utilization of M-BDSs*

3-Φ Buck-Boost CSI Modulation 1/2

- *Monolithic Bidir. Bipolar GaN Switches Featuring 2 Gates → Full Controllability*
- *Buck-Stage for Impressing Const. DC Current / PWM of CSI for Output Voltage Control*

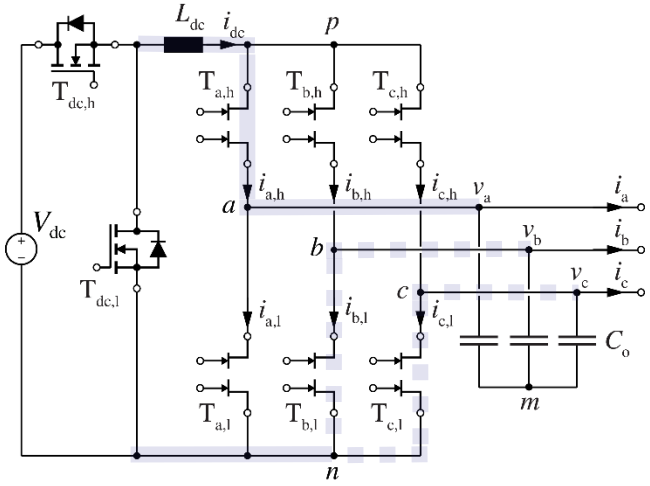


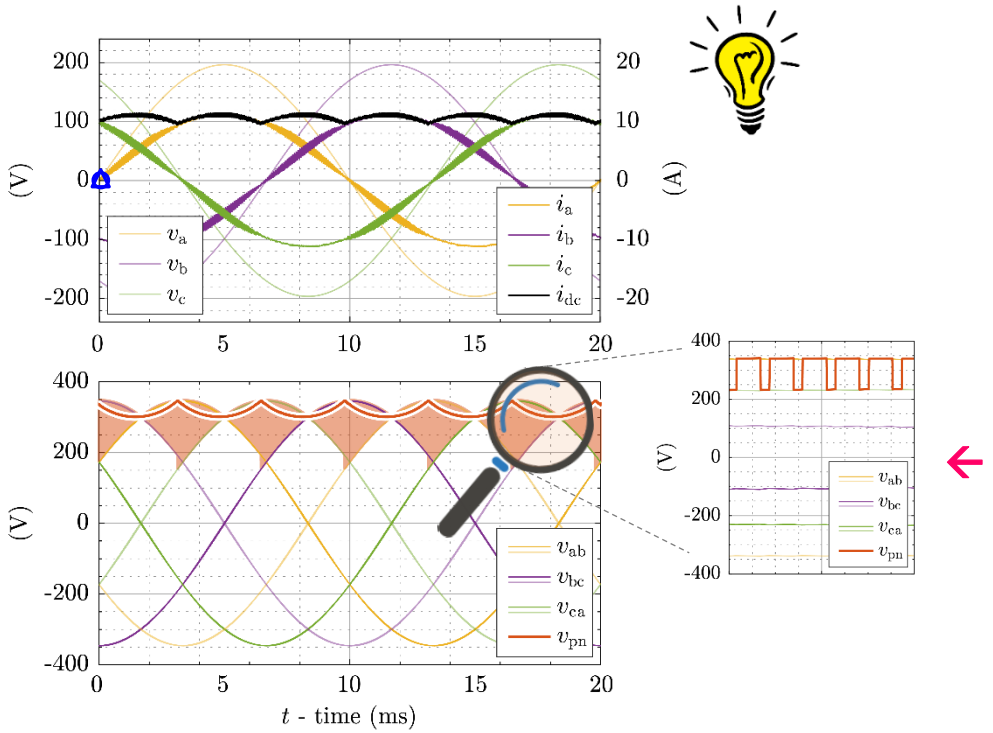


- *Conventional Control of Inverter Stage → Switching of All 3 Phase Legs (3/3)*

3-Φ Buck-Boost CSI Modulation 2/2

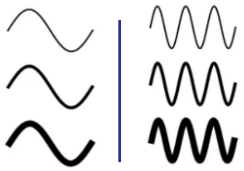
- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of One CSI-Phase*





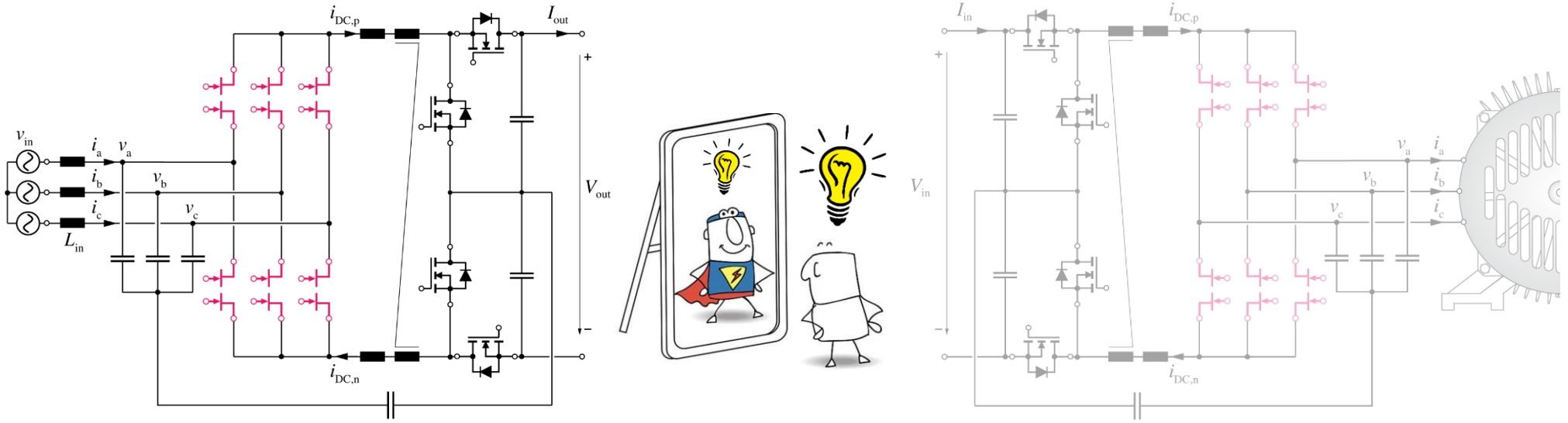
- *Switching of Only 2 of 3 Phase Legs (2/3 Mode) → Significant Reduction of Sw. Losses*

3-Φ AC/AC Conversion



Derivation of 3-Φ Current Source AC/AC Converter 1/2

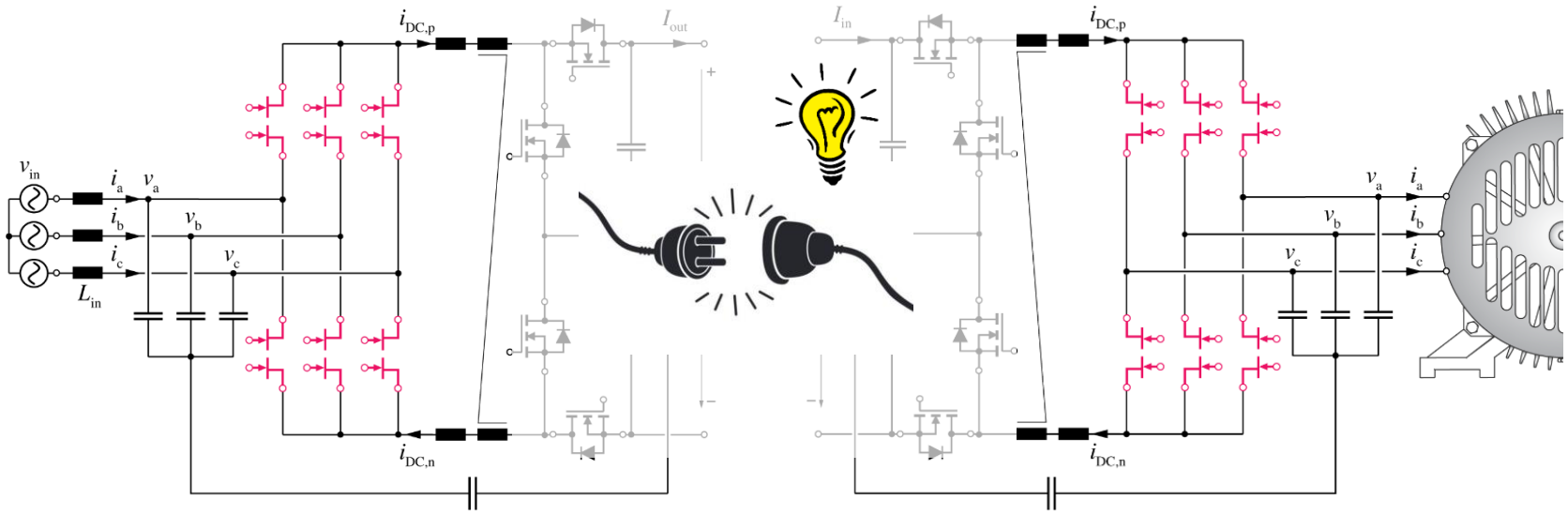
- *Derivation Based on Bidir. Buck-Boost Current Source Inverter (CSI) → Buck-Boost PFC Rectifier*
- *Lower # of Ind. Components Compared to Boost-Buck Rectifier Approach*



- *AC/DC Buck Stage Distributes DC-Link Current to Mains Phases — Sinusoidal Inp. Current*
- *Synergetic Control/Modulation of Rectifier Stage & DC/DC Stage for Min. Sw. Losses*

Derivation of 3-Φ Current Source AC/AC Converter 2/2

- *DC-Side Coupling of Buck-Boost Current DC-Link PFC Rectifier & Inverter — AC/DC/AC*
- *Full-Sinewave Filtering @ Input & Output w/ Single Magnetic Component*

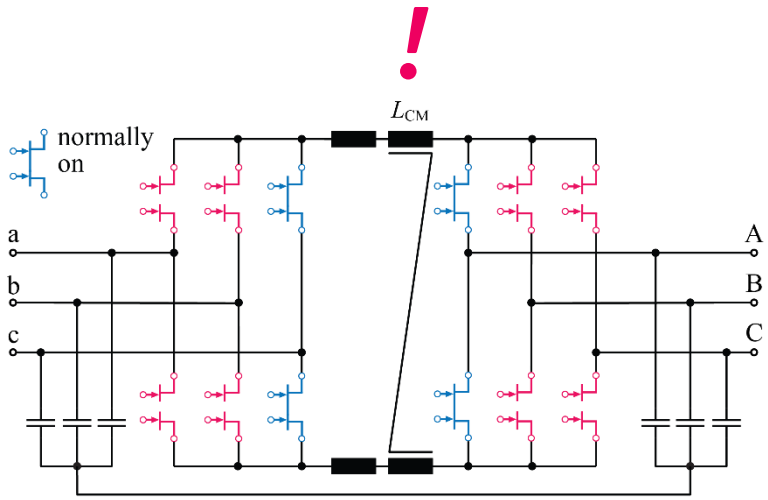


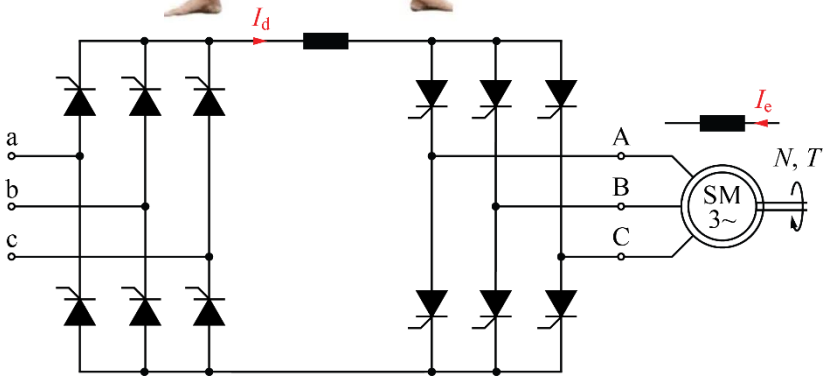
- *Bipolar Blocking / Unidir. Switches | Unidir. DC-Link Current Sufficient for Bidir. Power Conversion*
- *Modulation-Based Inversion of DC-Link Voltage Polarity → Inv. of Power Flow Direction*

3-Φ Current Source AC/AC Converter

- *Sinusoidal Motor Voltage Achieved w/ Single Ind. Component*
- *Unidir. Valves Sufficient for Bidir. Power Conversion*
- *M-BDSs — Synchronous Rectification*

Source: www.mb-drive-services.com



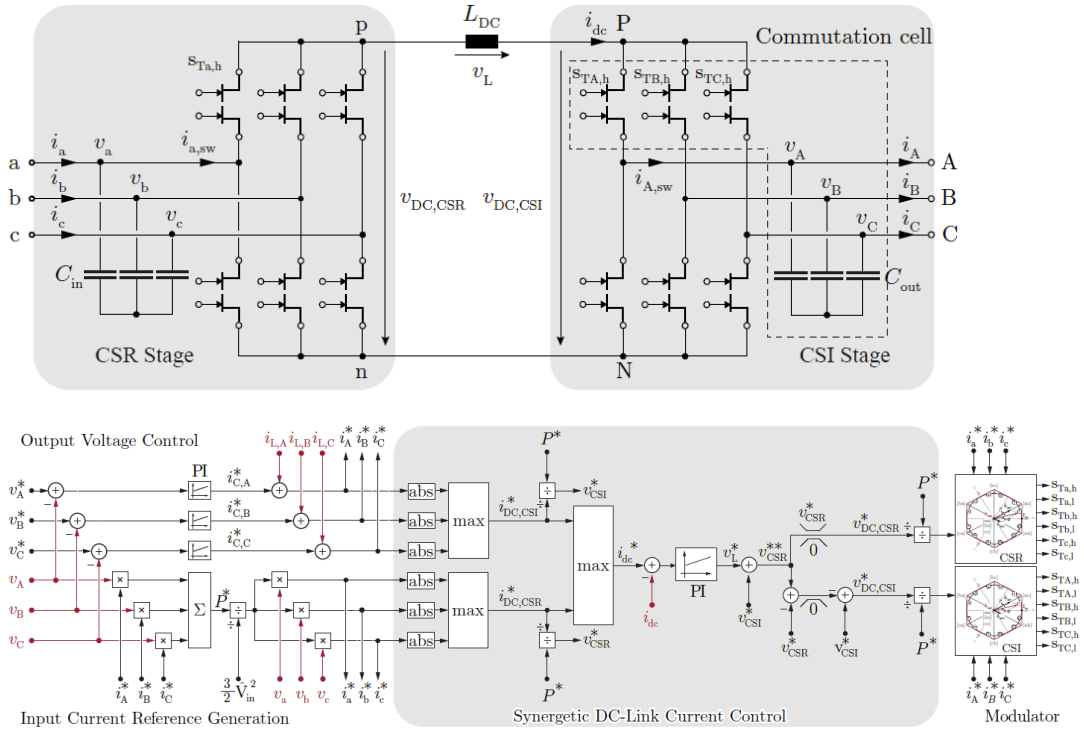


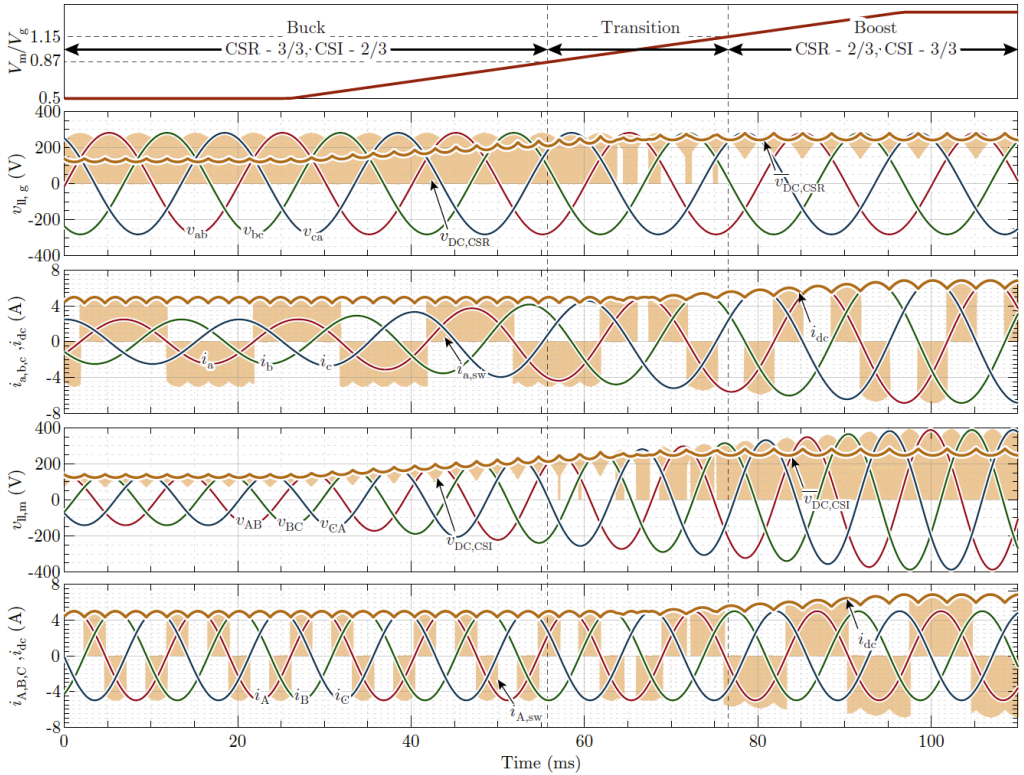
- *Relation to High-Power Thyristor-Based Medium-Voltage Synchr. Machine Variable Speed Drives*

Synergetic Control

Synergetic Control of 3-Φ AC/AC CSC

- *CSR-Stage OR CSI-Stage Continuously Operates with 2/3-PWM | Seamless Transition*

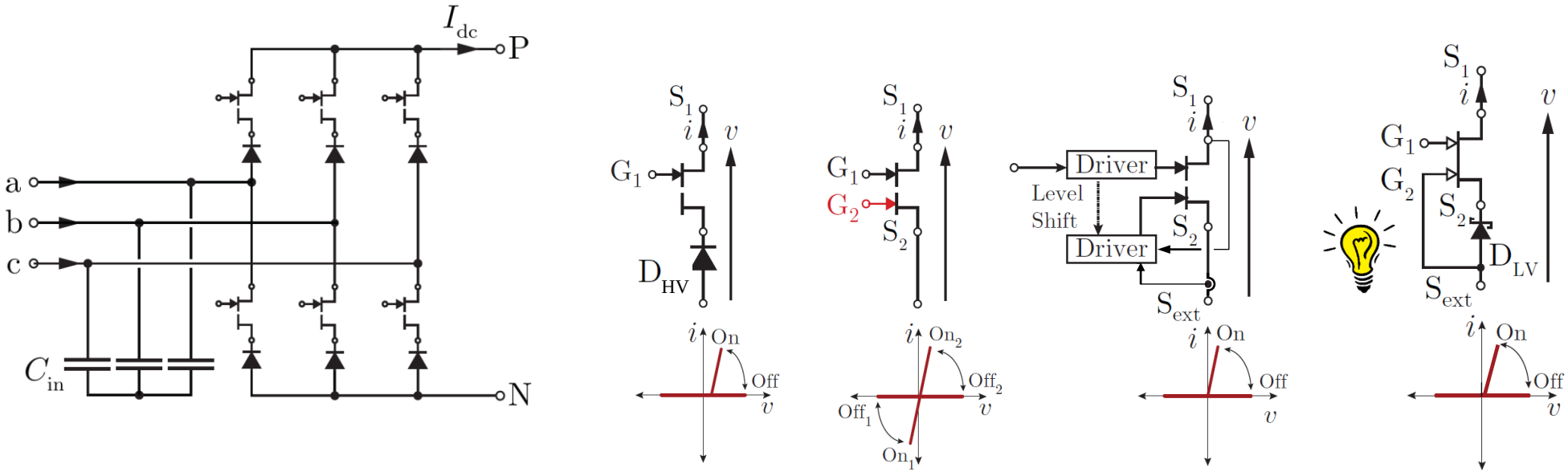




- *Buck-Mode → CSR-Stage Shapes DC-Link Current — 2/3 PWM of CSI-Stage*
- *Boost-Mode → CSI-Stage Shapes DC-link Current — 2/3 PWM of CSR-Stage*

Remark Self Reverse-Blocking M-BDS-Concept 1/2

- *Bidir. Curr. DC-Link Converters — Unidir. I_{dc} & Bipolar U_{dc} OR Bidir. I_{dc} & Unipolar U_{dc}*
  - *HV Switch + HV Diode* — *HV Diode Characteristic / High Cond. Losses*
  - *M-BDS* — *Ohmic Cond. Char. BUT 2 External Gate Signals / 2 Gate Drivers*
  - *"Self-Switching"* — *Ohmic Cond. Char. BUT High Local Complexity (Sensing)*

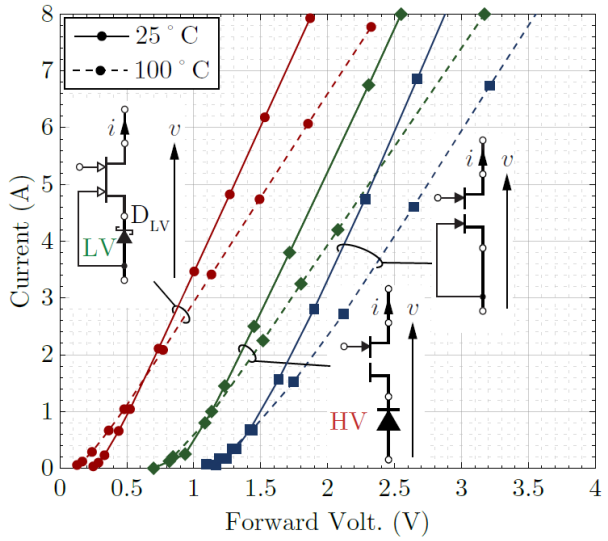


- *SRB-MBDS* — *Quasi-Ohmic Cond. Char. (Cascode w/ LV Si Schottky Diode) & 1 External Gate*

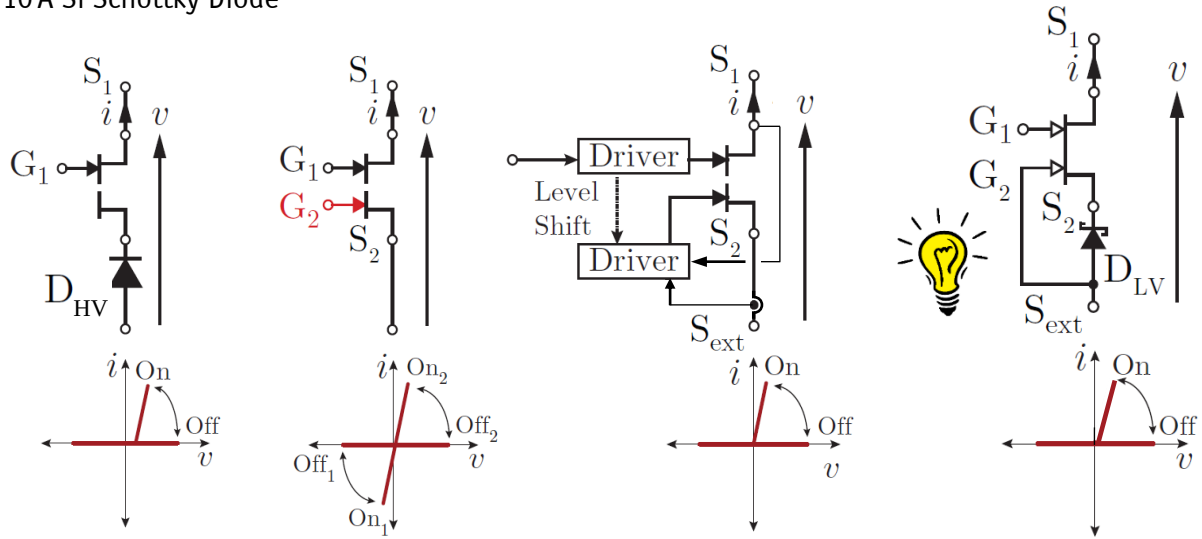
Remark Self Reverse-Blocking M-BDS-Concept 2/2

■ *Bidir. Curr. DC-Link Converters — Unidir. I_{dc} & Bipolar U_{dc} OR Bidir. I_{dc} & Unipolar U_{dc}*

- *HV Switch + HV Diode* — *HV Diode Characteristic / High Cond. Losses*
- *M-BDS* — *Ohmic Cond. Char. BUT 2 External Gate Signals / 2 Gate Drivers*
- *"Self-Switching"* — *Ohmic Cond. Char. BUT High Local Complexity (Sensing)*



600 V 190 mΩ GaN M-BDS
40 V/10 A Si Schottky Diode



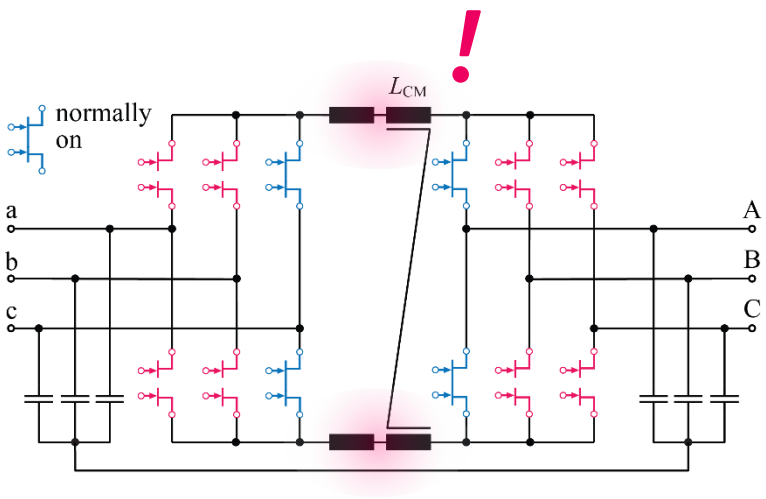
- *SRB-MBDS* — *Quasi-Ohmic Cond. Char. (Cascode w/ LV Si Schottky Diode) & 1 External Gate*

Source: www.reuts.com

DUALITY

■ Current DC-Link Topology

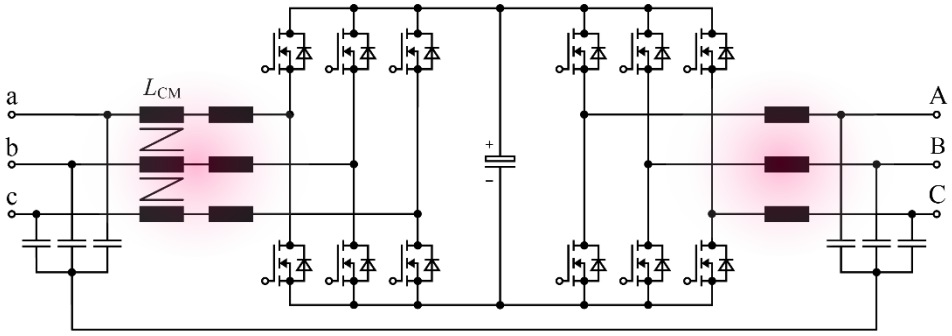
- Application of M-BDSs
- Complex 4-Step Commutation OR SRB-MBDSs
- Low Filter Volume



- Challenging Overvoltage Protection
- Limited Control Dynamics

■ Voltage DC-Link Topology

- Standard Bridge-Legs
- Low-Complexity Commutation
- Defined Semiconductor Voltage Stress
- Facilitates DC-Link Energy Storage

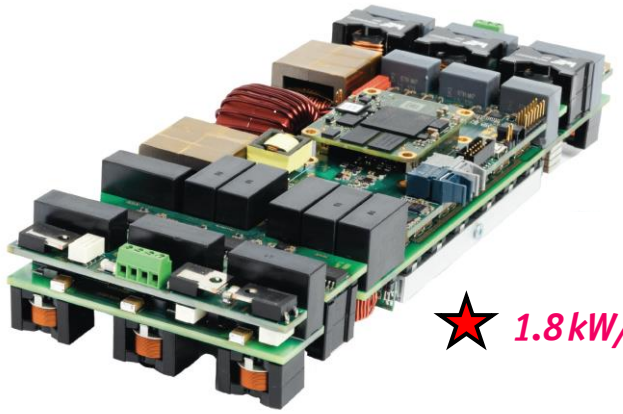


- High Input / Output Filter Volume

DUALITY

■ Current DC-Link Topology

- Application of M-BDSs
- Complex 4-Step Commutation
- Low Filter Volume



★ 1.8 kW/dm³

■ Voltage DC-Link Topology

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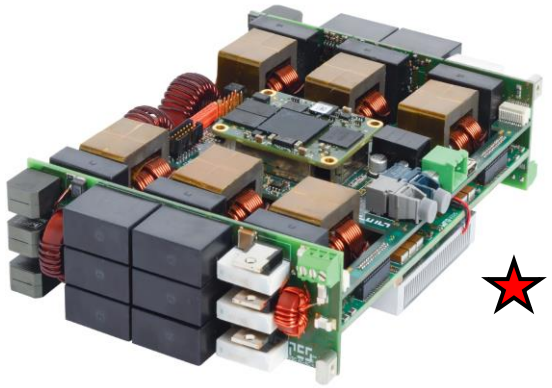
- Low-Complexity Commutation
- Defined Semiconductor Voltage Stress
- Facilitates DC-Link Energy Storage



★ 1.7 kW/dm³

■ All-600V-GaN AC-AC VSDs / 1.4 kW, 200V L-L / Full EMI Filter (Grid & Motor) / 97% Nominal Eff.

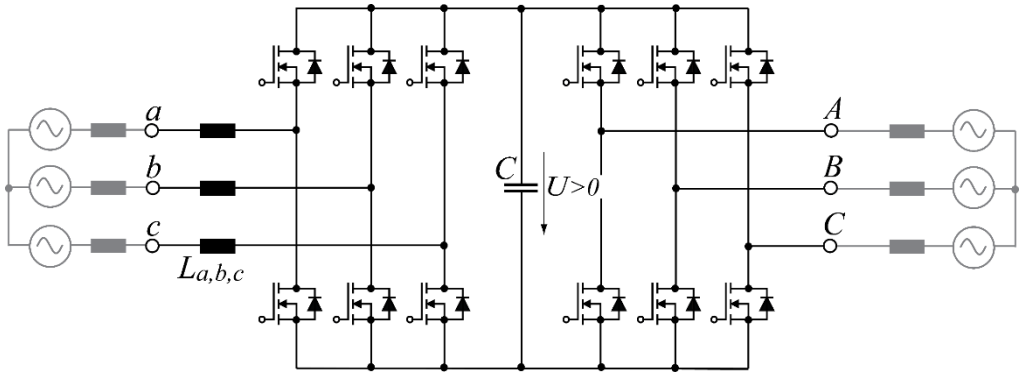
3-Φ AC/AC
Matrix Converter

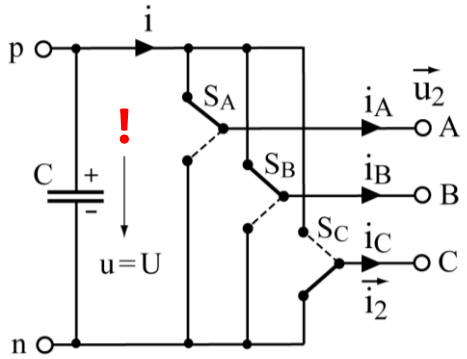
3-Φ Voltage Source Converter
Space Vector Based Analysis

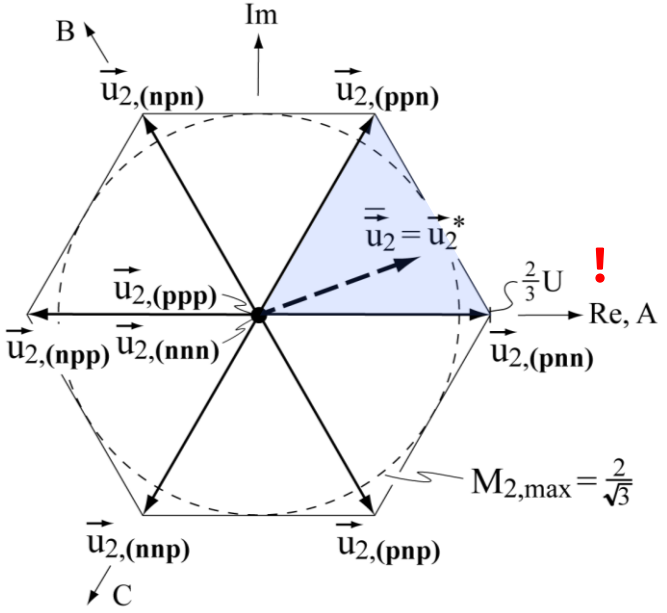
VSC Space Vector Modulation 1/2

- *Switching Considering Interlock Delay Times*
- *2^3 = 8 Switching States*

$$\vec{u}_{2,j} = \frac{2}{3}\left(u_{A,j} + \underline{a}u_{B,j} + \underline{a}^2 u_{C,j}\right) \qquad \vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$$



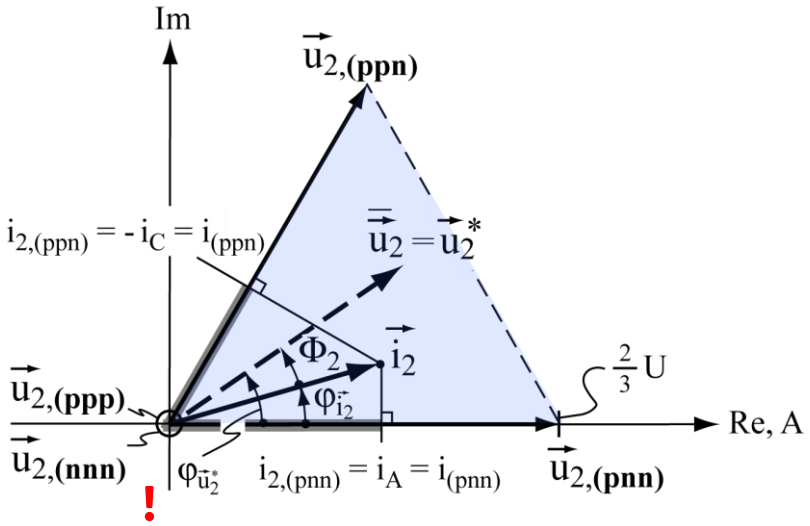




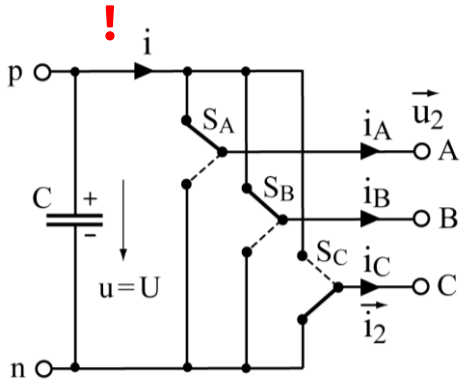
- *Continuous OR Discontinuous Modulation → (nnn)-(pnn)-(ppn)-(ppp) OR (nnn)-(pnn)-(ppn)*

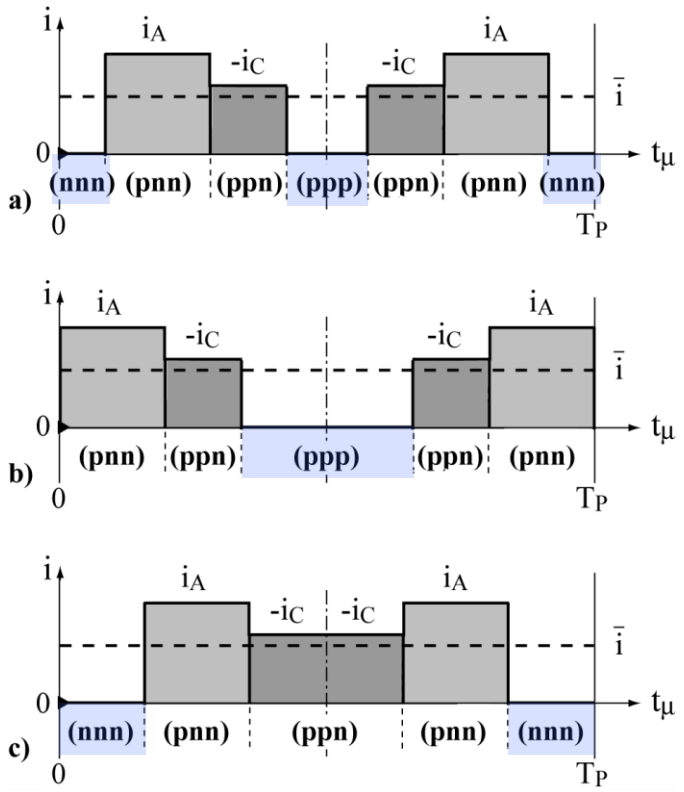
VSC Space Vector Modulation 2/2

- *Switching Considering Interlock Delay Times*
- *2^3 = 8 Switching States*



$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2$$

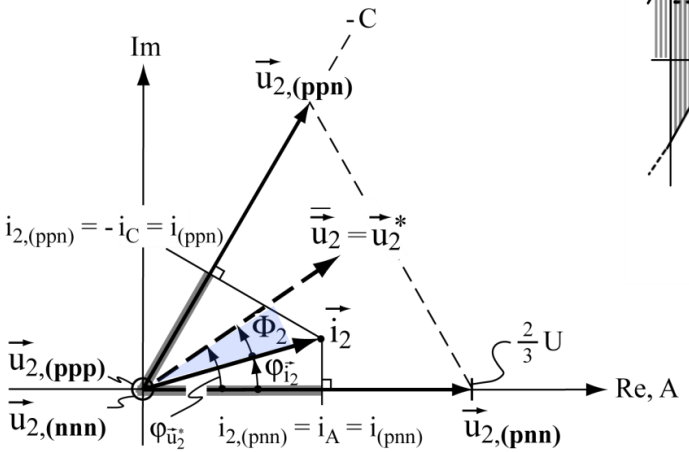


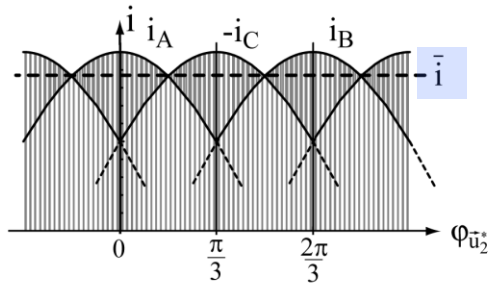


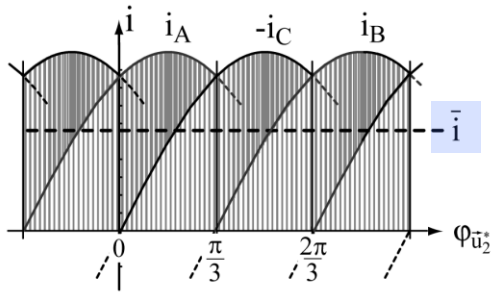
- *Continuous OR Discontinuous Modulation → (nnn)-(pnn)-(ppn)-(ppp) OR (nnn)-(pnn)-(ppn)*

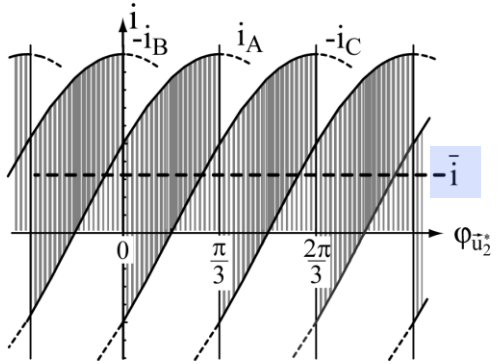
VSI DC-Link Current Waveform

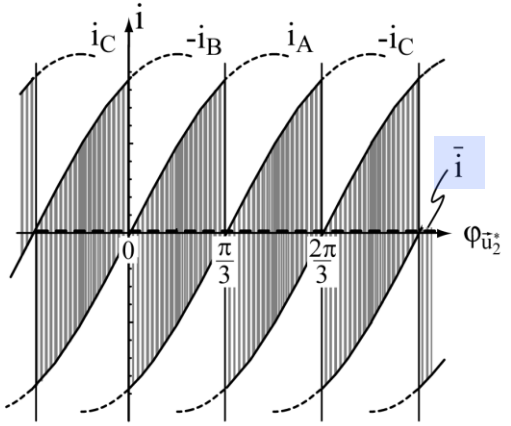
Influence of Output Voltage Phase Displacement Φ_2 on DC-link Current Waveform









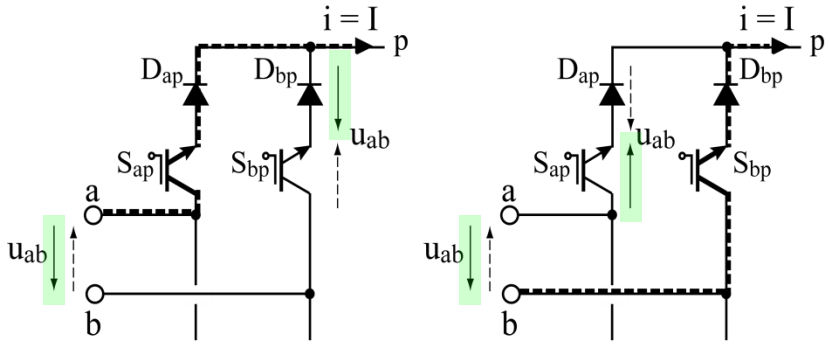


$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2 \qquad M_2 = 2/\sqrt{3}$$

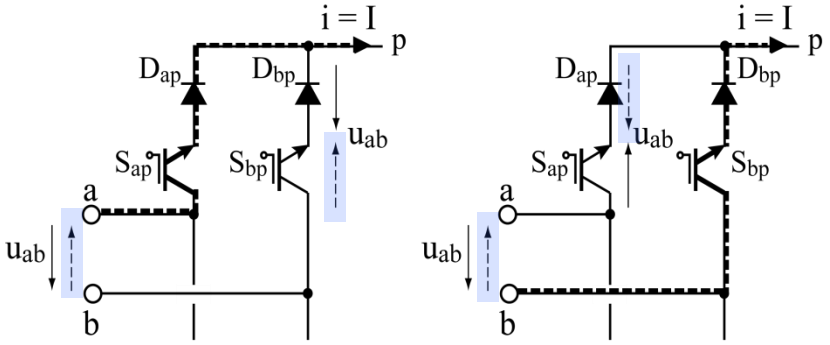
3-Φ Current Source Converter
Space Vector Based Analysis

CSR Commutation & Equivalent Circuit

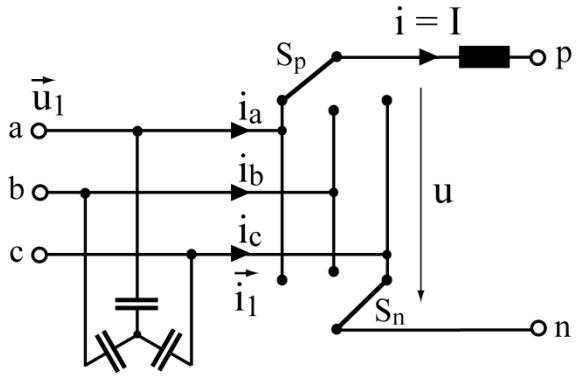
Forced Commutation



Natural Commutation



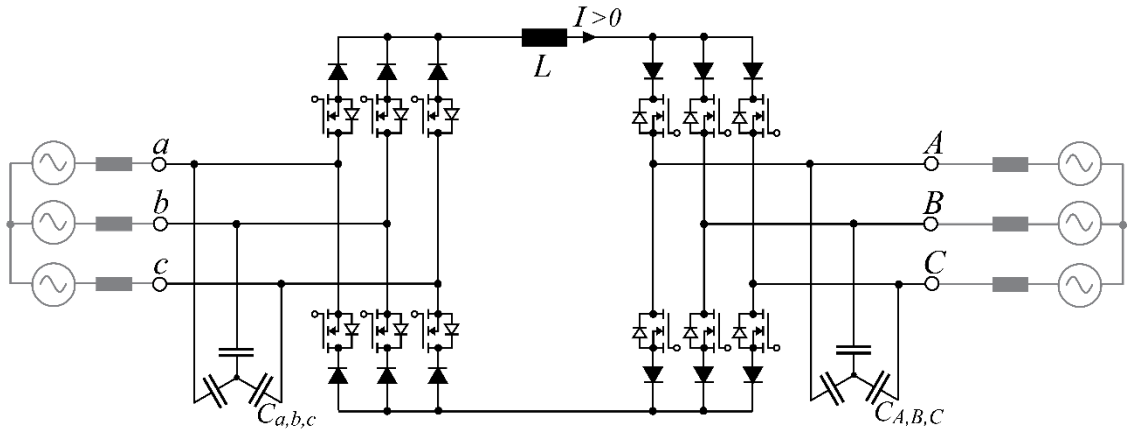
Equivalent Circuit

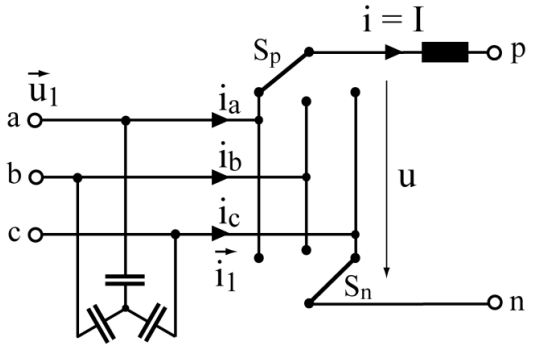


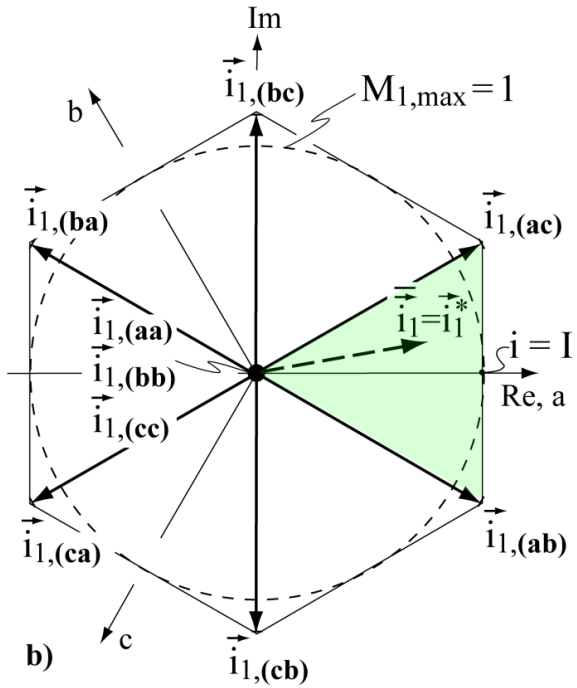
CSC Space Vector Modulation 1/2

- *Overlapping Switching → Natural or Forced Commutation*
- *$3^2 = 9$ Switching States*

$$\vec{i}_k = \frac{2}{3}\left(i_{a,k} + \underline{a}\, i_{b,k} + \underline{a}^2\, i_{c,k}\right) \qquad \vec{i}_1^{\,*} = \hat{I}_1^* e^{j\varphi_{\vec{i}_1}} = \hat{I}_1^* e^{j(\omega_1 t - \Phi_1^*)}$$



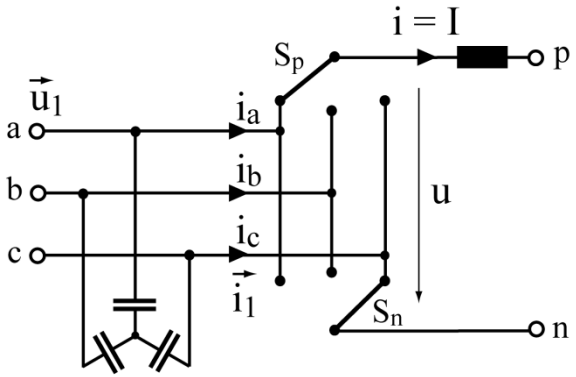




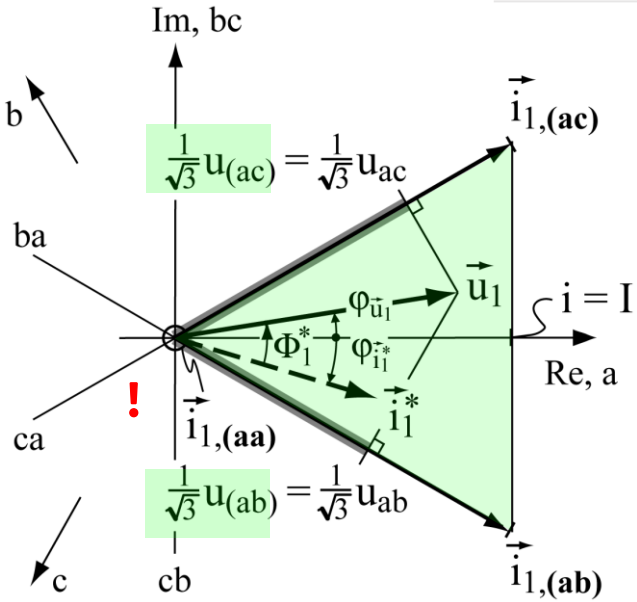
- *Shoot-Trough Free-Wheeling States (aa), (bb), (cc) → i_a=i_b=i_c=0*

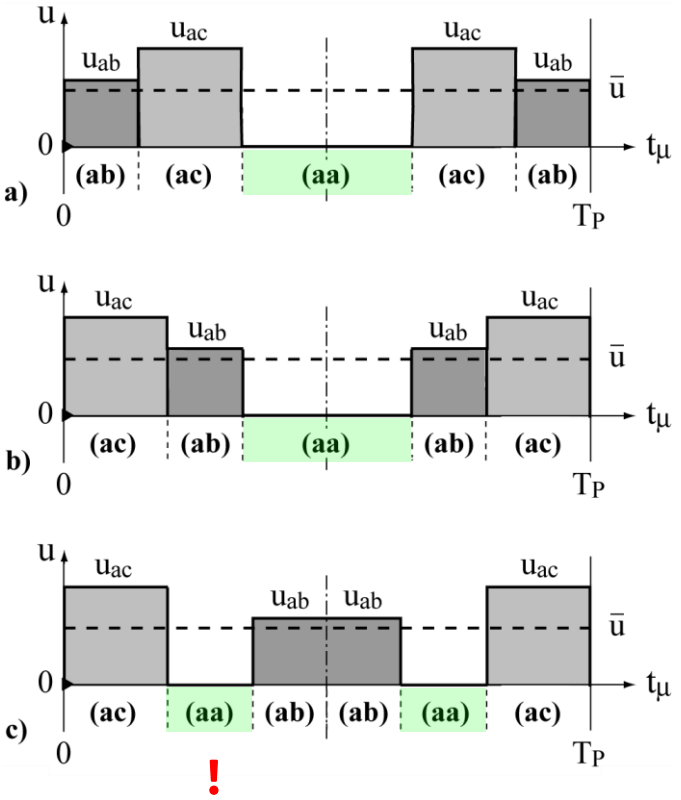
CSC Space Vector Modulation 2/2

- *Overlapping Switching → Natural or Forced Commutation*
- *3^2 = 9 Switching States*



$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

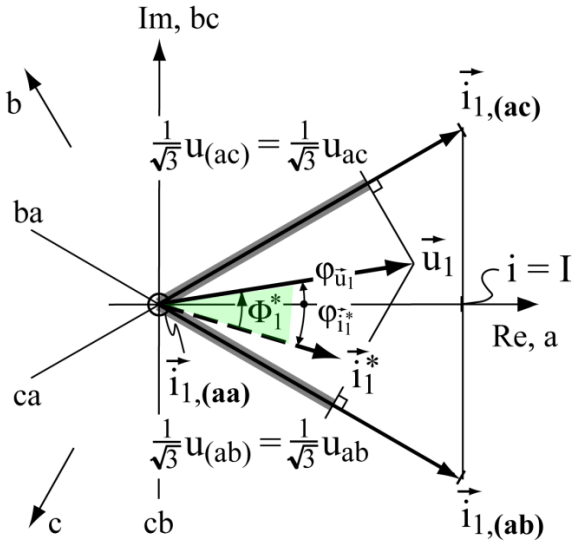


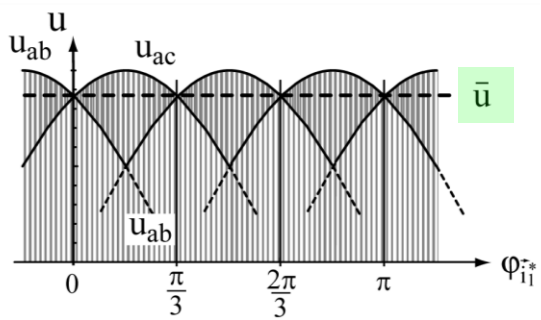


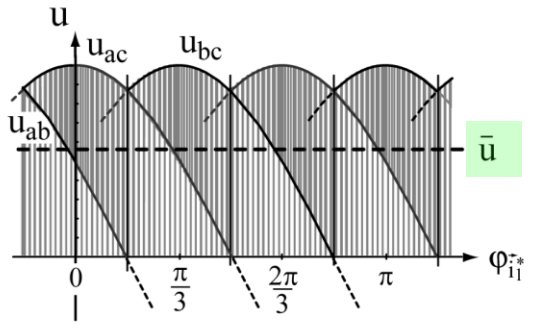
- *Shoot-Trough Free-Wheeling States (aa), (bb), (cc) → i_a=i_b=i_c=0*

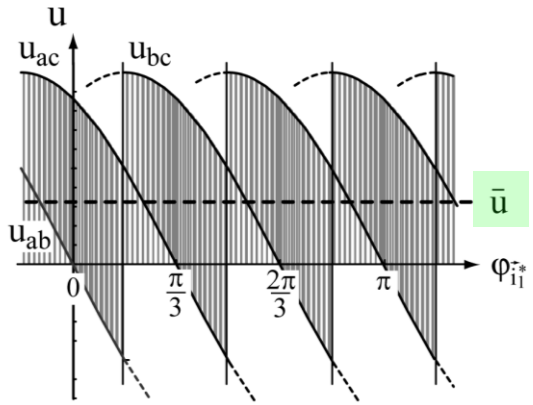
CSR DC-Link Voltage Waveform

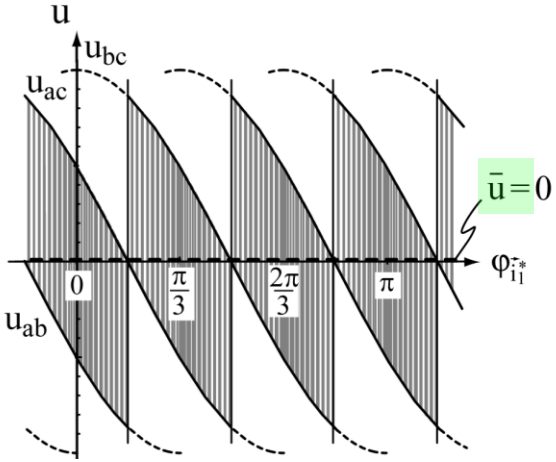
Influence of Input Current Phase Displacement Φ_1 on DC-link Voltage Waveform











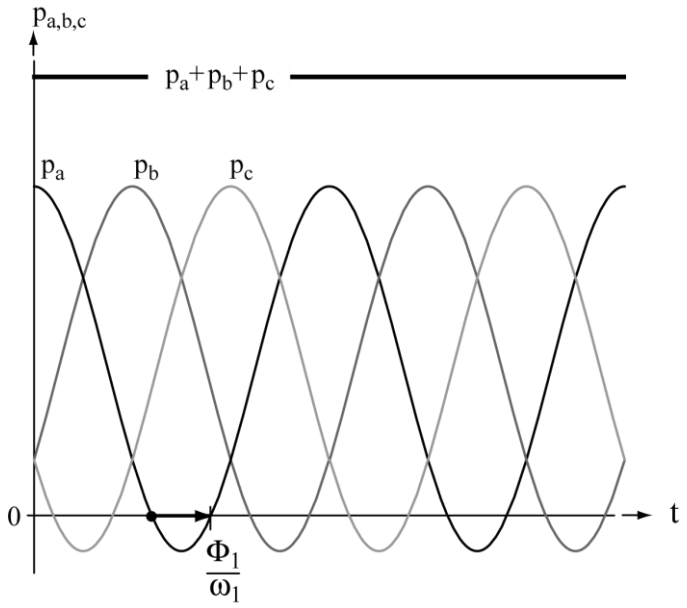
$$M_1 = \frac{\hat{I}_1^*}{I}$$

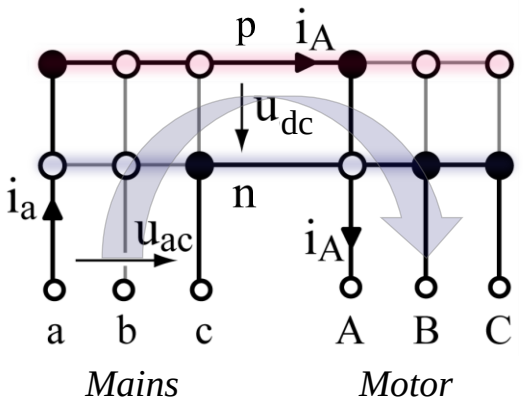
!

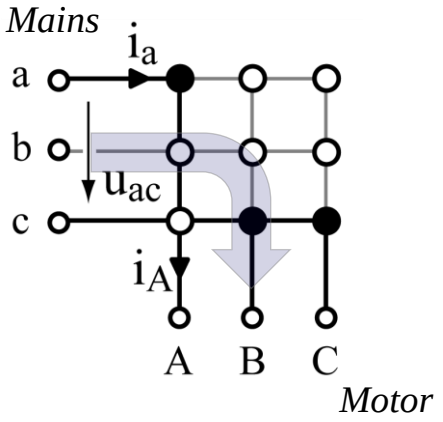
$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

Indirect & Direct 3-Φ AC/AC Matrix Converter

- *Constant 3-Φ Instantaneous Power Flow → No Low-Frequ. DC-Link Power Pulsation Buffer Requirement (!)*
- *Indirect AC/DC—DC/AC OR Direct AC/AC Power Conversion → IMC OR DMC*
- *DMC → Switch Matrix w/ Bipolar Voltage Blocking & Current Carrying Devices*



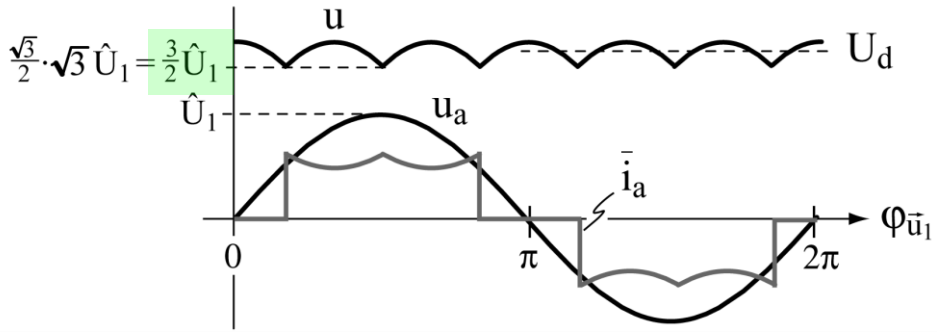




- *Input-Side Cap. / Output-Side Motor Ind. → Operation Limited to Buck-Type (Step-Down) Conversion*

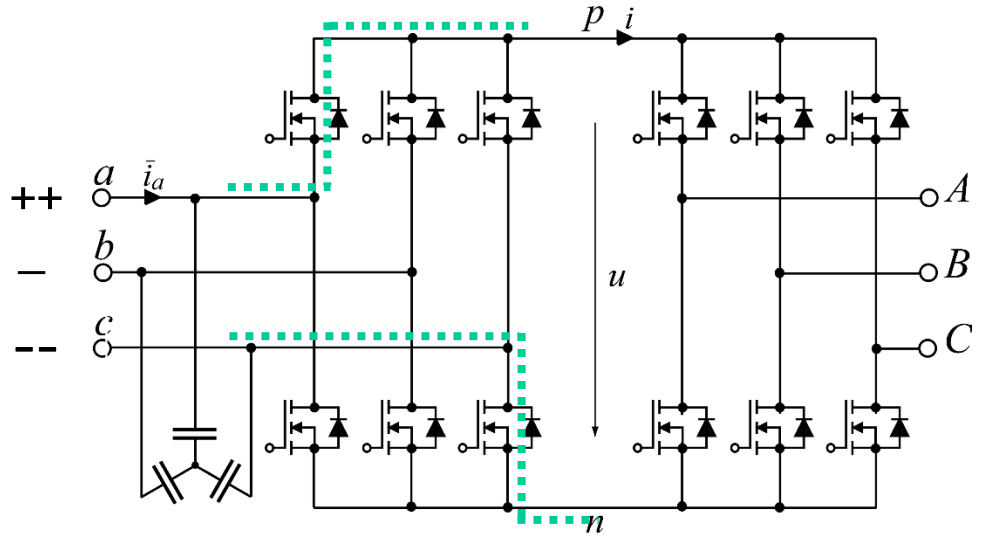
Fundamental Frequency Front-End (F³E)

- *Voltage DC-Link AC/AC Converter w/o Energy Storage*
- *Input Diode Bridge w/ Antiparallel Transistors → Regenerative Braking*



$$u_{\min} = \frac{3}{2}\hat{U}_1 \qquad !$$

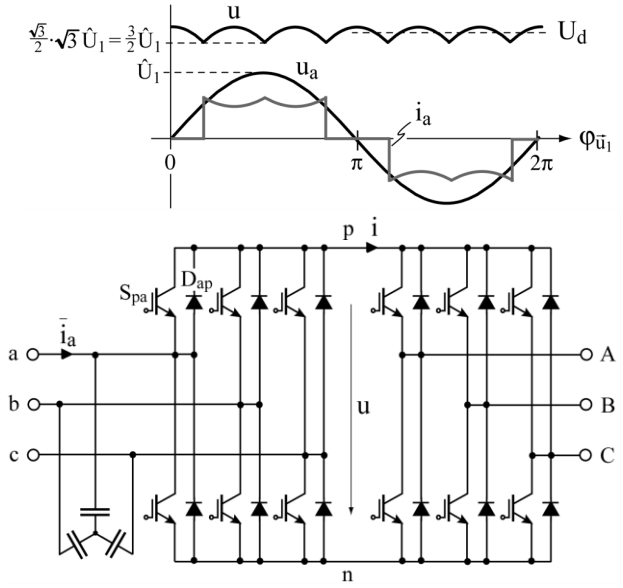
$$\hat{U}_2^* < \frac{\sqrt{3}}{2}\cdot\hat{U}_1 \approx 0.86\,\hat{U}_1$$

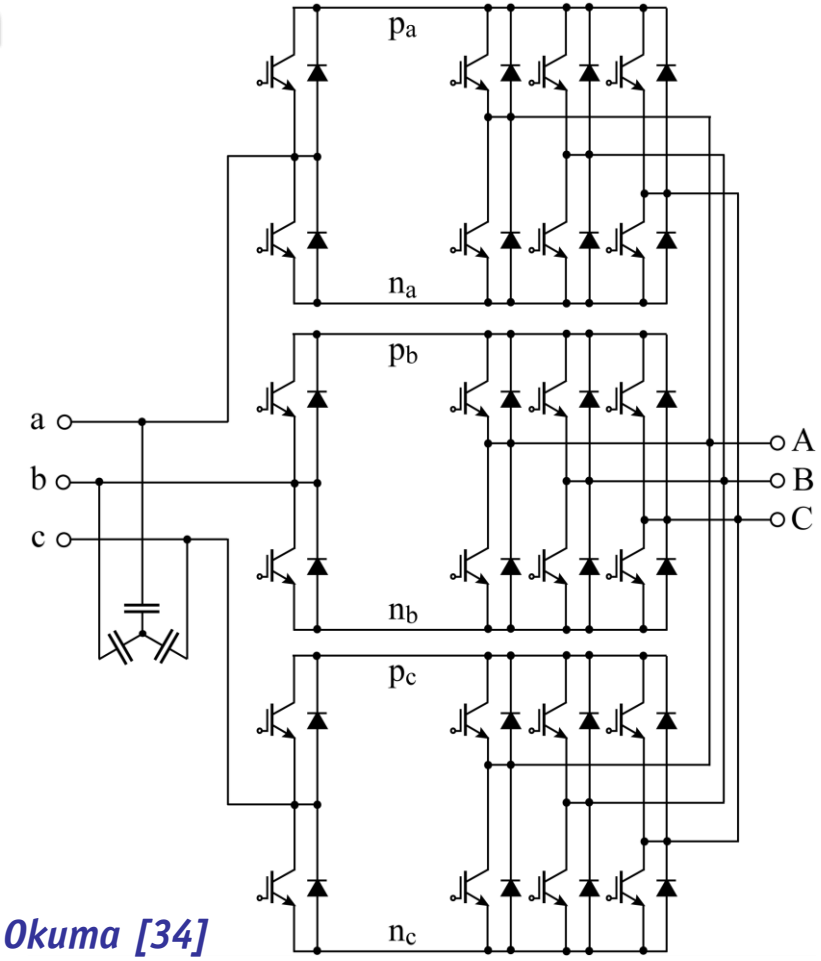


- *Limited Output Voltage Range*
- *Diodes Determine Switching State of Mains Interface → Block-Shaped Mains Current*

F³E Topology Extension

- *Sinusoidal Mains Current*





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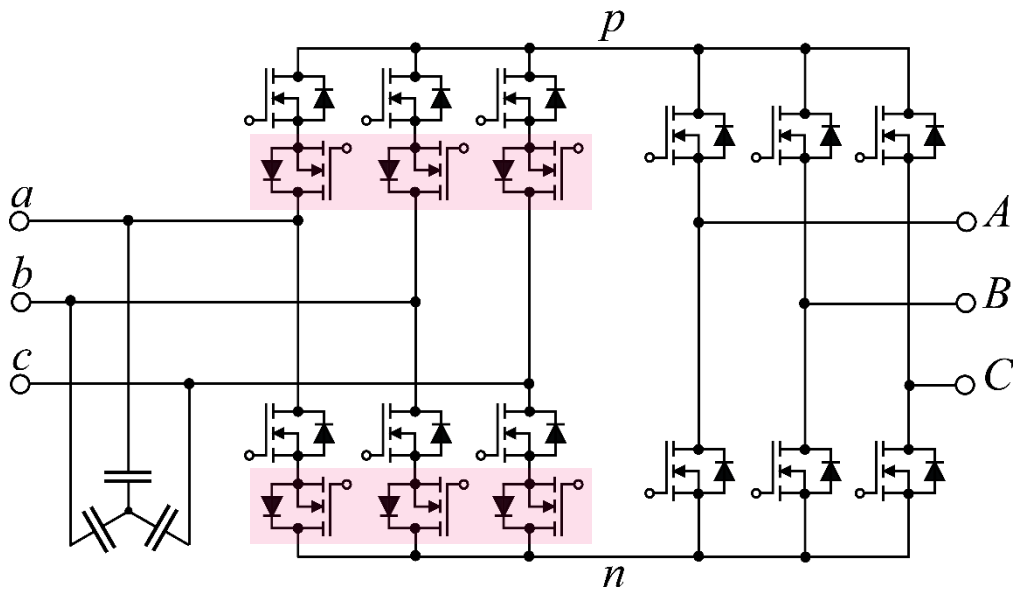
Indirect Matrix Converter (IMC)

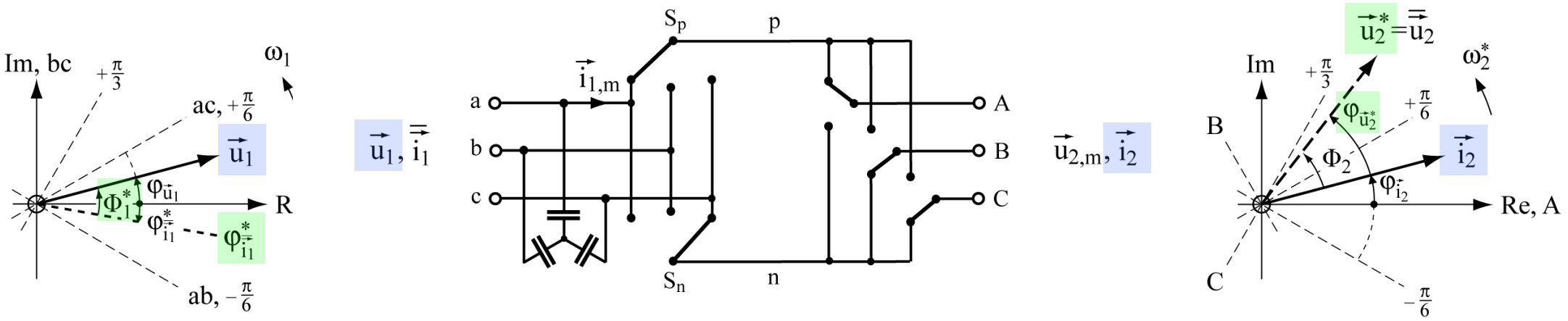
- *Extension of the F³E-Topology → AC Switches / Full Controllability of Mains Interface*
- *Sinusoidal Mains Current*



- *Positive DC-Link Voltage Mandatory !*
- *Coordinated PWM of Input & Output Stage*

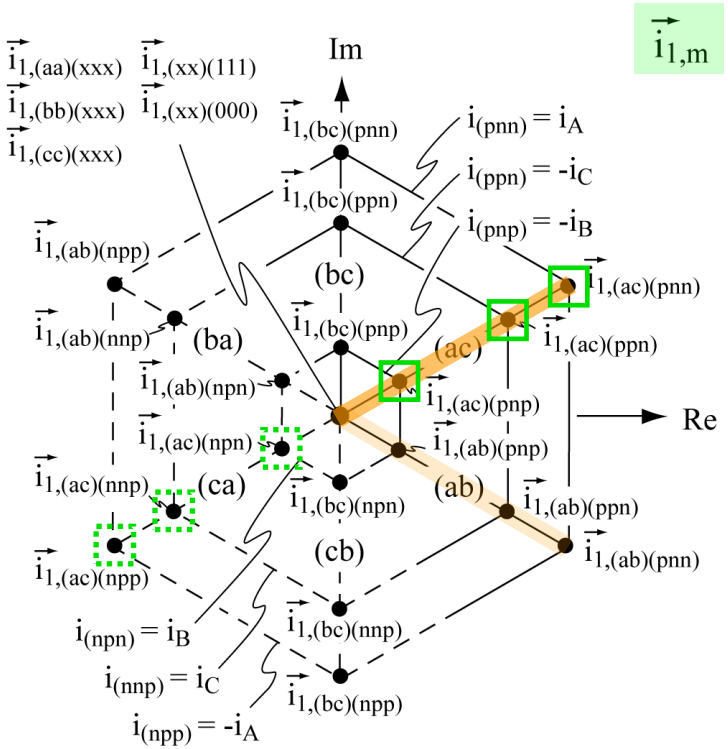
IMC Space Vector Modulation

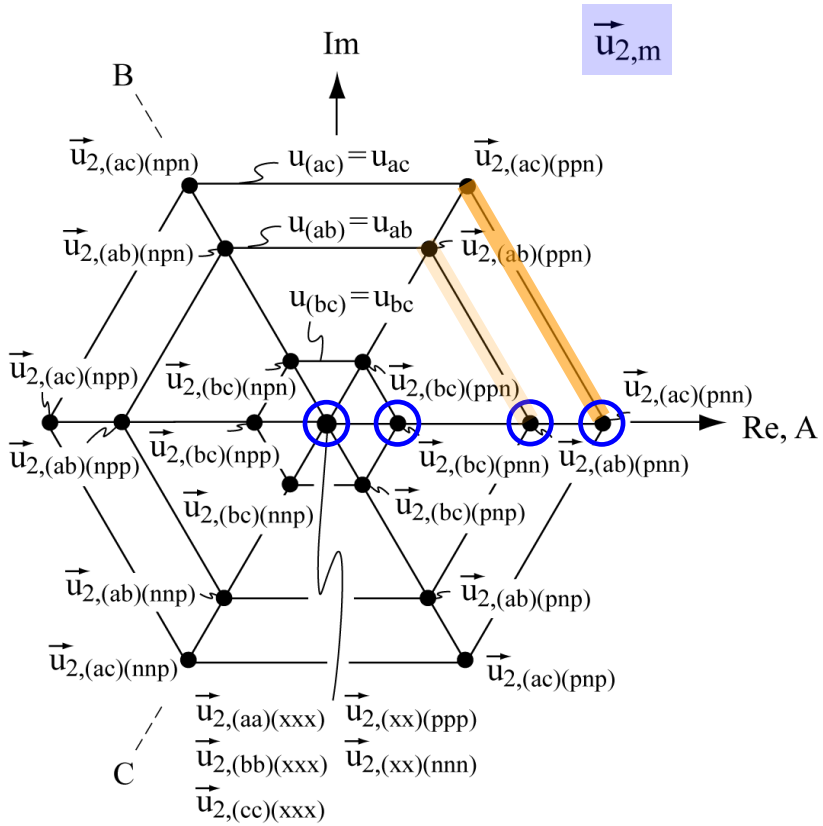
- *Hybrid Voltage DC-Link / Current DC-Link Converter*
- *Positive DC-Link Voltage Mandatory !*



- *DC-Link Voltage → Defined by Mains Line-to-Line Voltage Sections*
- *DC-Link Current → Defined by Load/Motor Current Sections*

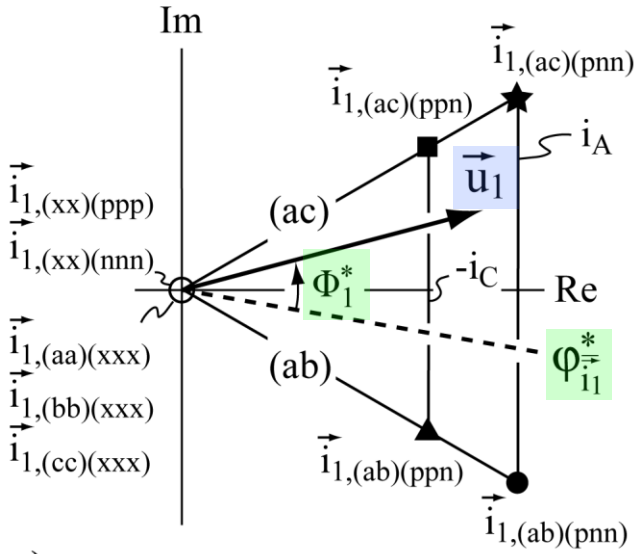
IMC Voltage & Current Space Vectors



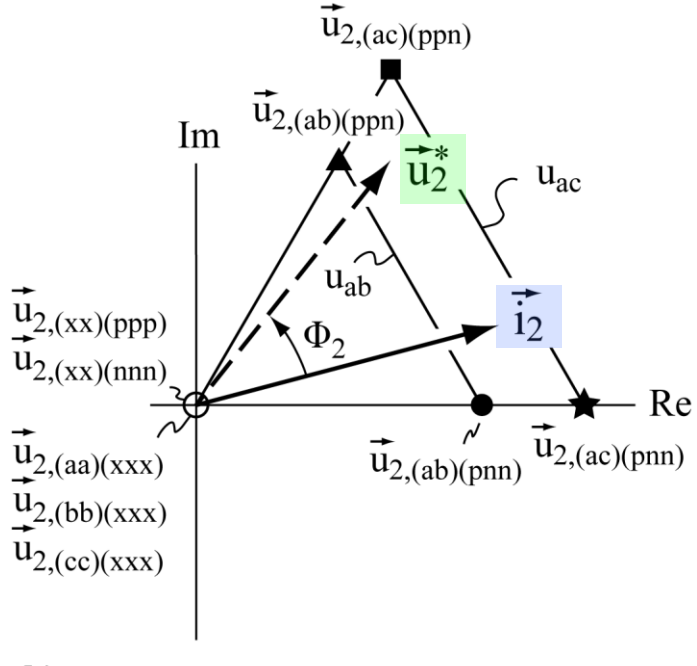


- *Positive DC-Link Voltage Mandatory !*
- *Coordinated PWM of Input & Output Stage*

IMC Space Vector Modulation



a)



b)

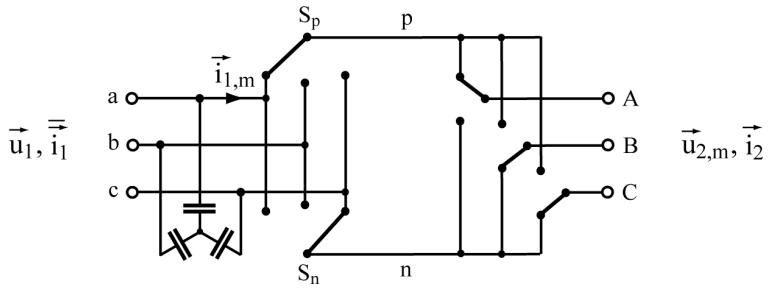
$$\vec{u}_1 = \hat{U}_1 e^{j\varphi_{\vec{u}_1}} = \hat{U}_1 e^{j\omega_1 t} \qquad \vec{i}_1 = \hat{I}_1 e^{j\varphi_{\vec{i}_1}^*}$$

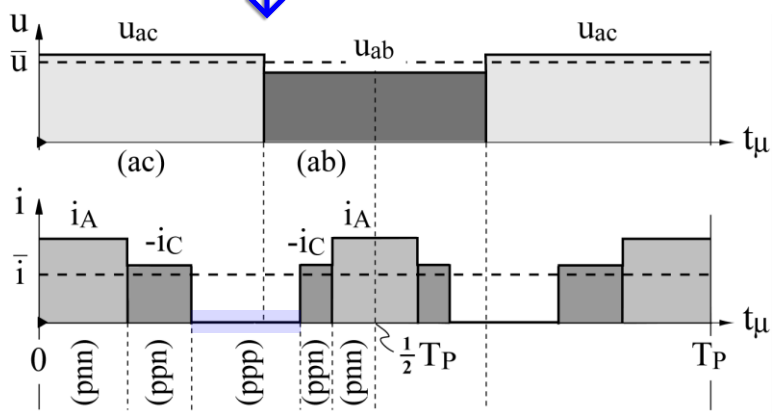
$$\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$$

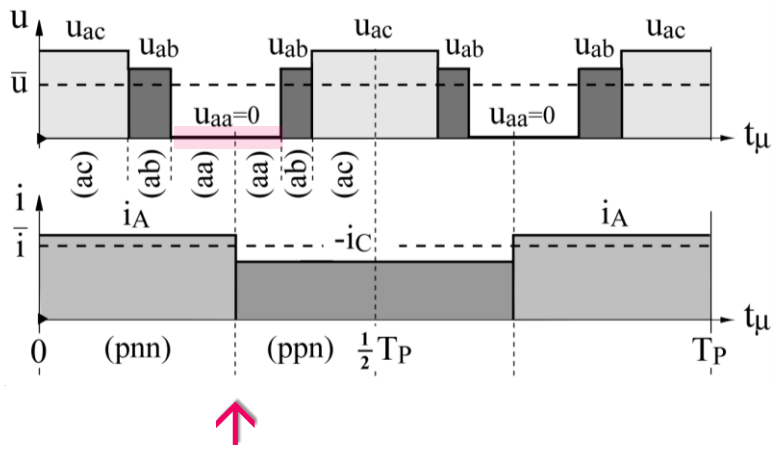
$$\vec{i}_2 = \hat{I}_2 e^{j\varphi_{\vec{i}_2}} = \hat{I}_2 e^{j\left(\varphi_{\vec{u}_2^*} - \Phi_2\right)}$$

IMC Commutation / Modulation

- *Hybrid Voltage DC-Link / Current DC-Link Converter*
- *Positive DC-Link Voltage Mandatory !*



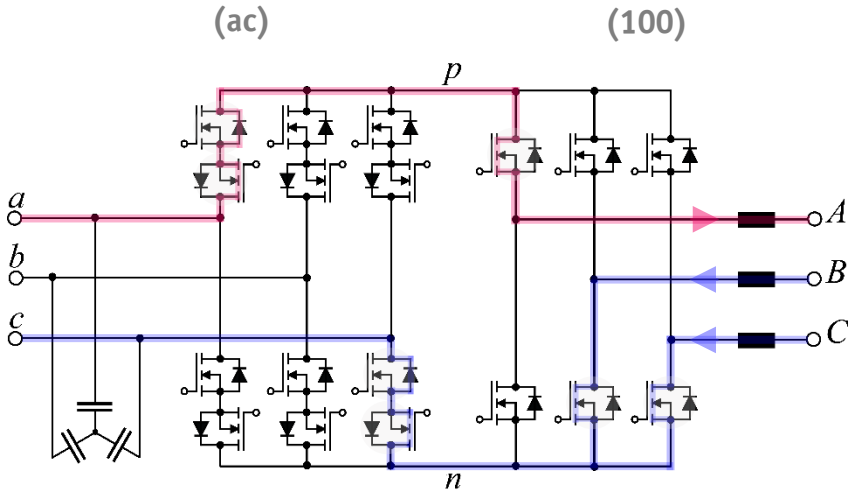


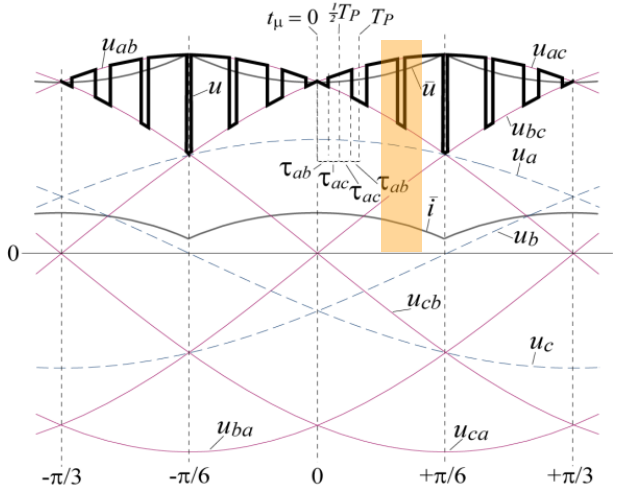


- *Zero Current Commutation of Input Stage*
- *Zero Voltage Commutation of Output Stage*

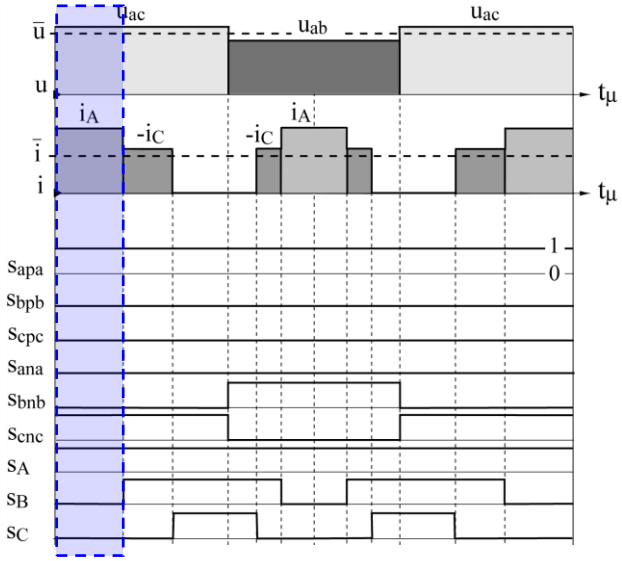
IMC Modulation 1/6

DC-link Voltage $u = u_{ac}$
DC-link Current $i = i_A$





120°of Mains Period

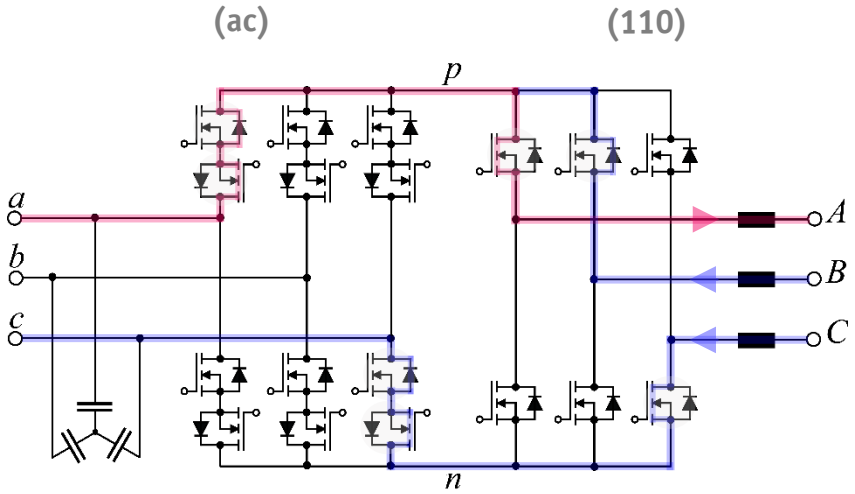


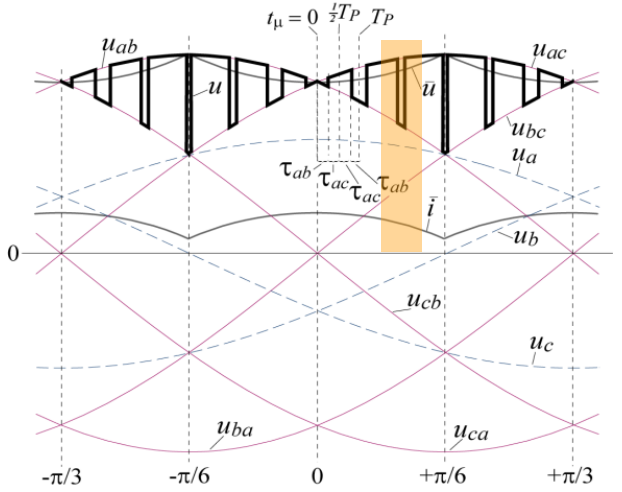
DC link Voltage & Current

PWM Pattern

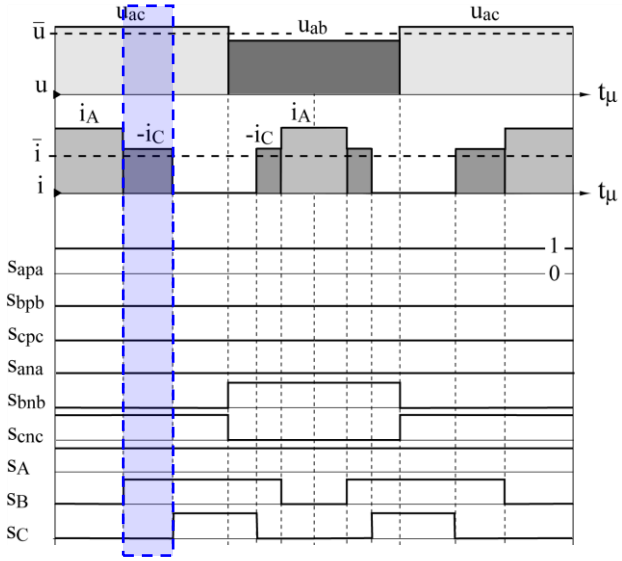
IMC Modulation 2/6

DC-link Voltage $u = u_{ac}$
DC-link Current $i = -i_C$





120° of Mains Period



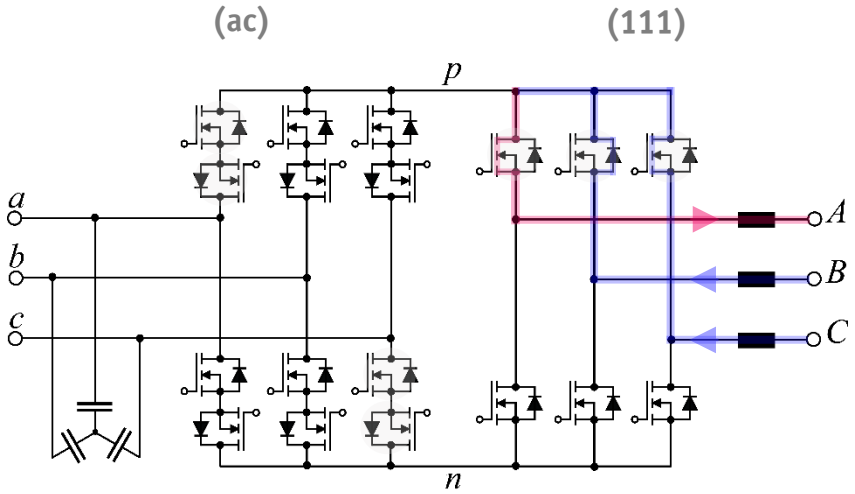
DC-Link Voltage & Current

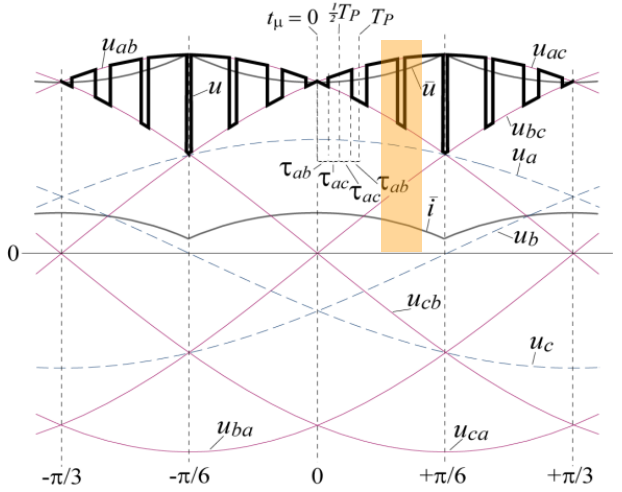
PWM Pattern

IMC Modulation 3/6

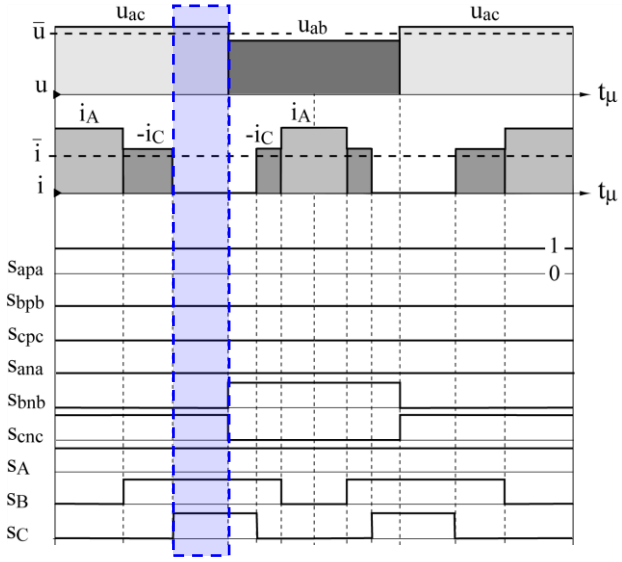
- *Input Stage Commutation @ i = 0*

DC-link Voltage $u = u_{ac}$
DC-link Current $i = 0$!





120° of Mains Period



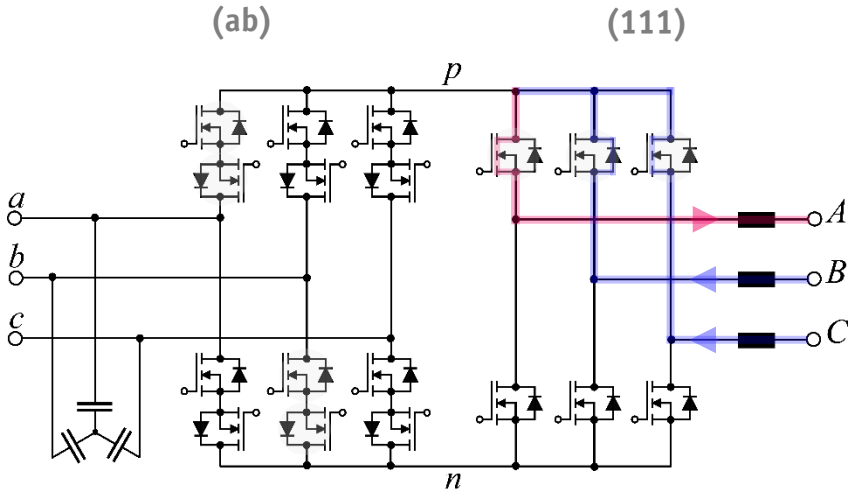
DC-Link Voltage & Current

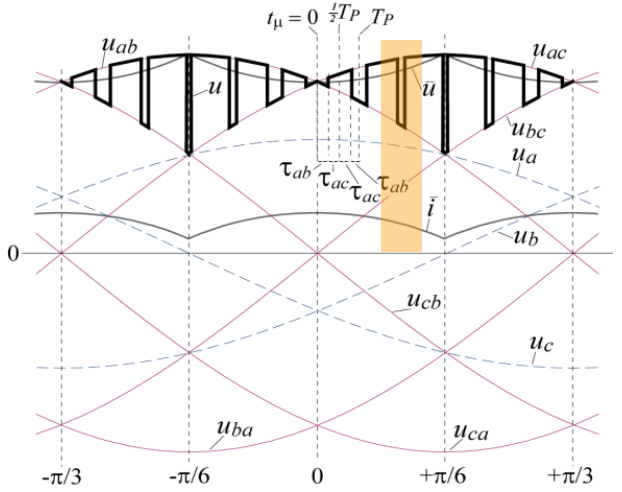
PWM Pattern

IMC Modulation 4/6

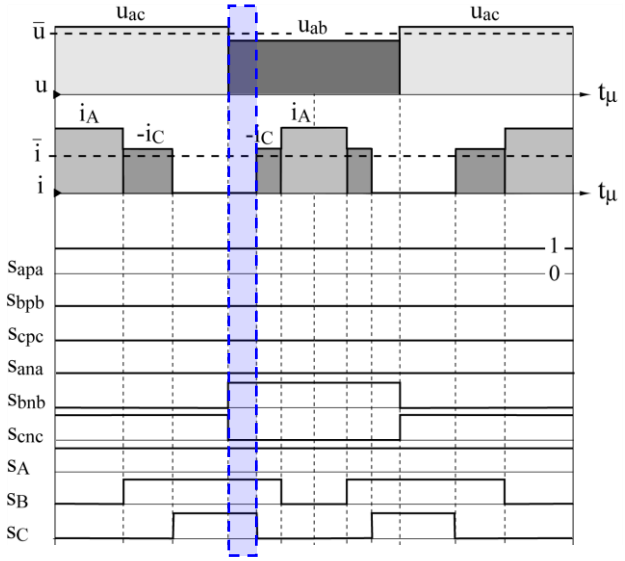
- *Input Stage Commutation @ i = 0*

DC-link Voltage $u = u_{ab}$
DC-link Current $i = 0$!





120° of Mains Period

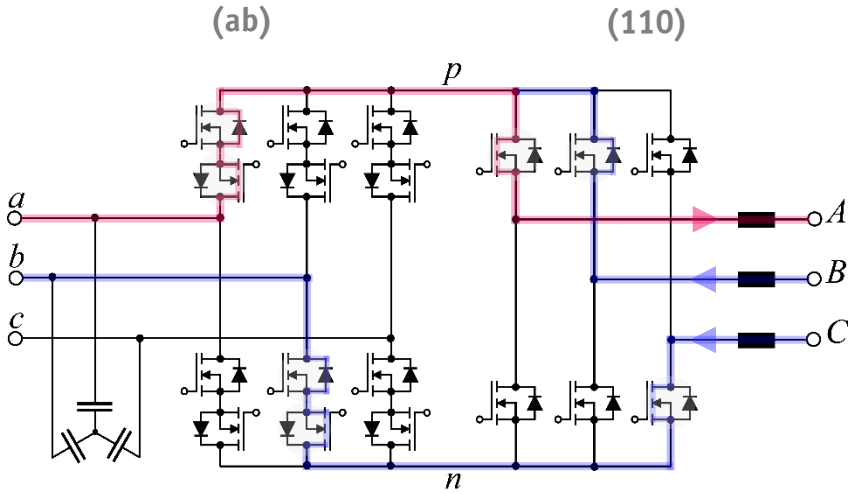


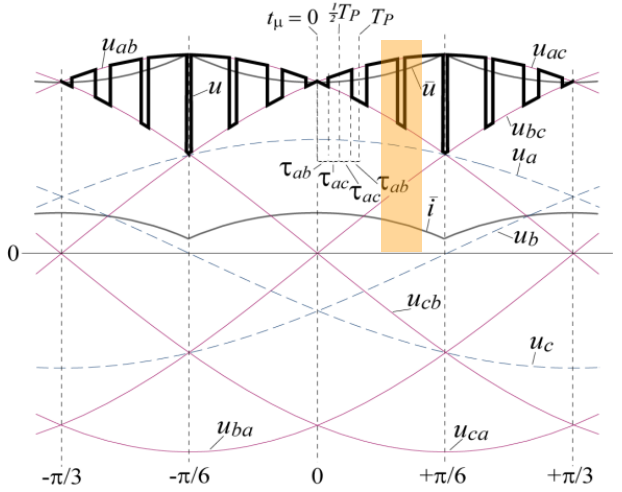
DC-Link Voltage & Current

PWM Pattern

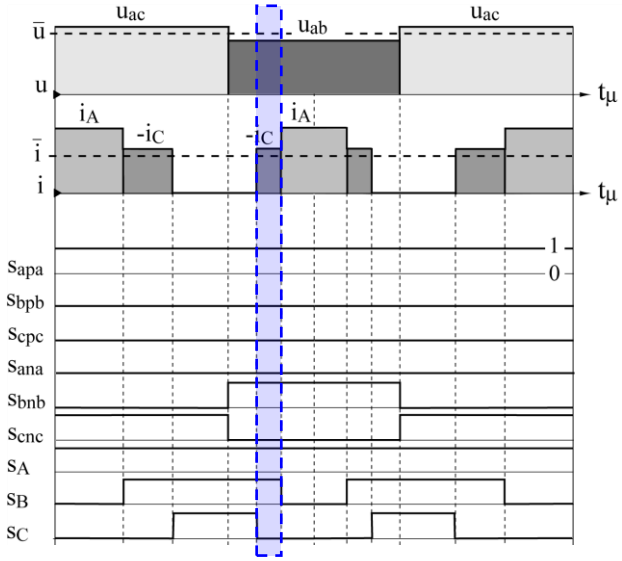
IMC Modulation 5/6

DC-link Voltage $u = u_{ab}$
DC-link Current $i = -i_C$





120°of Mains Period

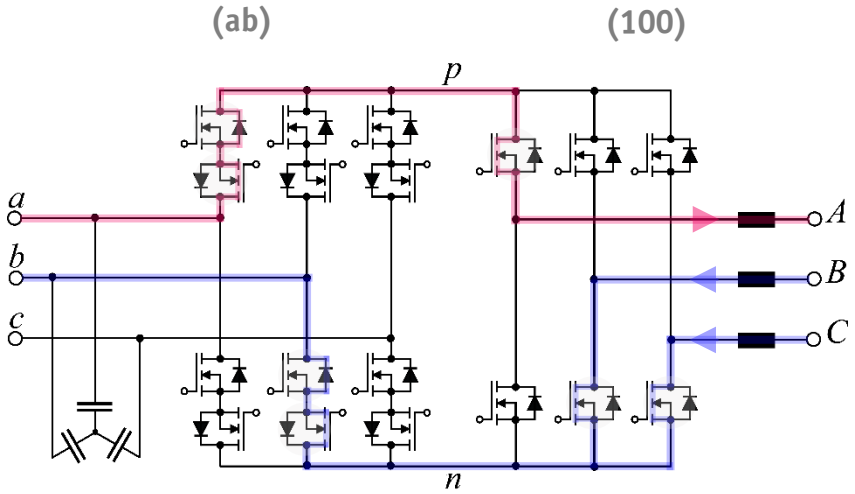


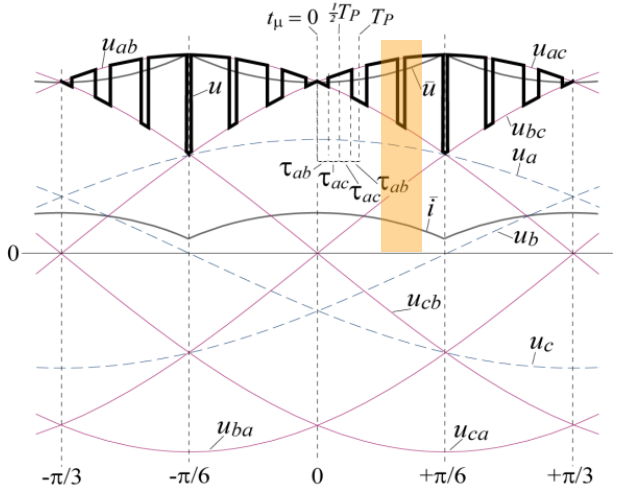
DC-Link Voltage & Current

PWM Pattern

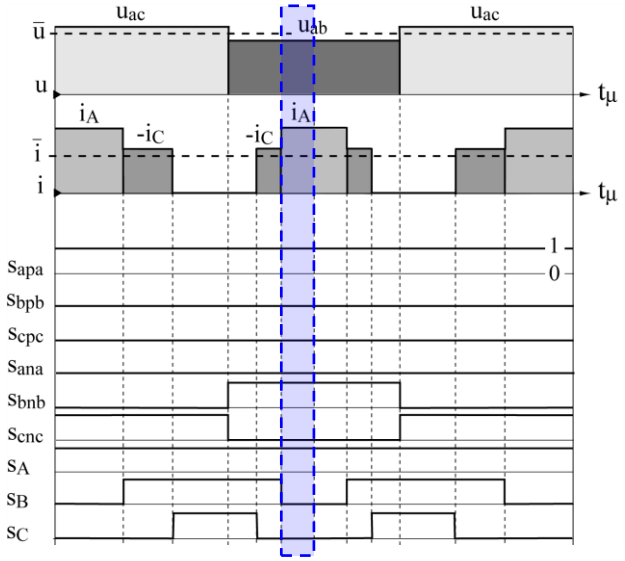
IMC Modulation 6/6

DC-link Voltage $u = u_{ab}$
DC-link Current $i = i_A$





120°of Mains Period



DC-Link Voltage & Current

PWM Pattern

Alternative Modulation Schemes 1/2

- *LV vs. HV Modulation*
  - *Lower Sw. Losses (40%) & Lower CM Voltage (25%)*
  - *Slightly Lower Load Current Ripple*
  - *Input Voltage Ripple Doubles (!)*
  - *Higher Conduction Losses*

- *High Output Voltage Modulation (HVM)*

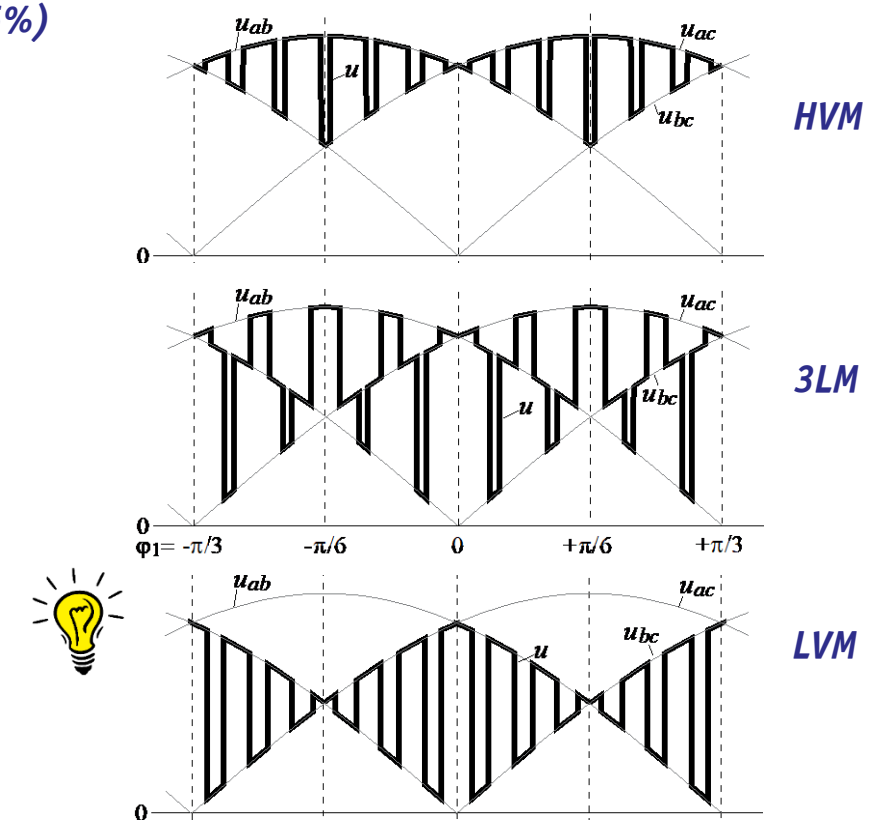
$$\hat{U}_2 = 0 \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

- *Three-Level Modulation (3LM)*

$$\hat{U}_2 = \frac{1}{2} \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

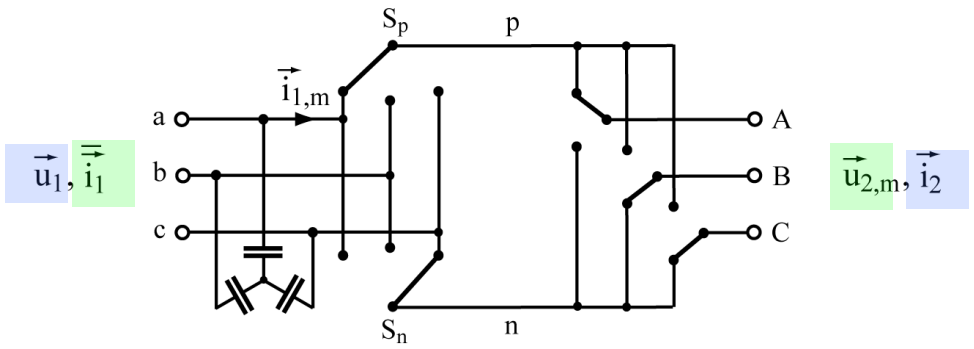
- *Low Output Voltage Modulation (LVM)*

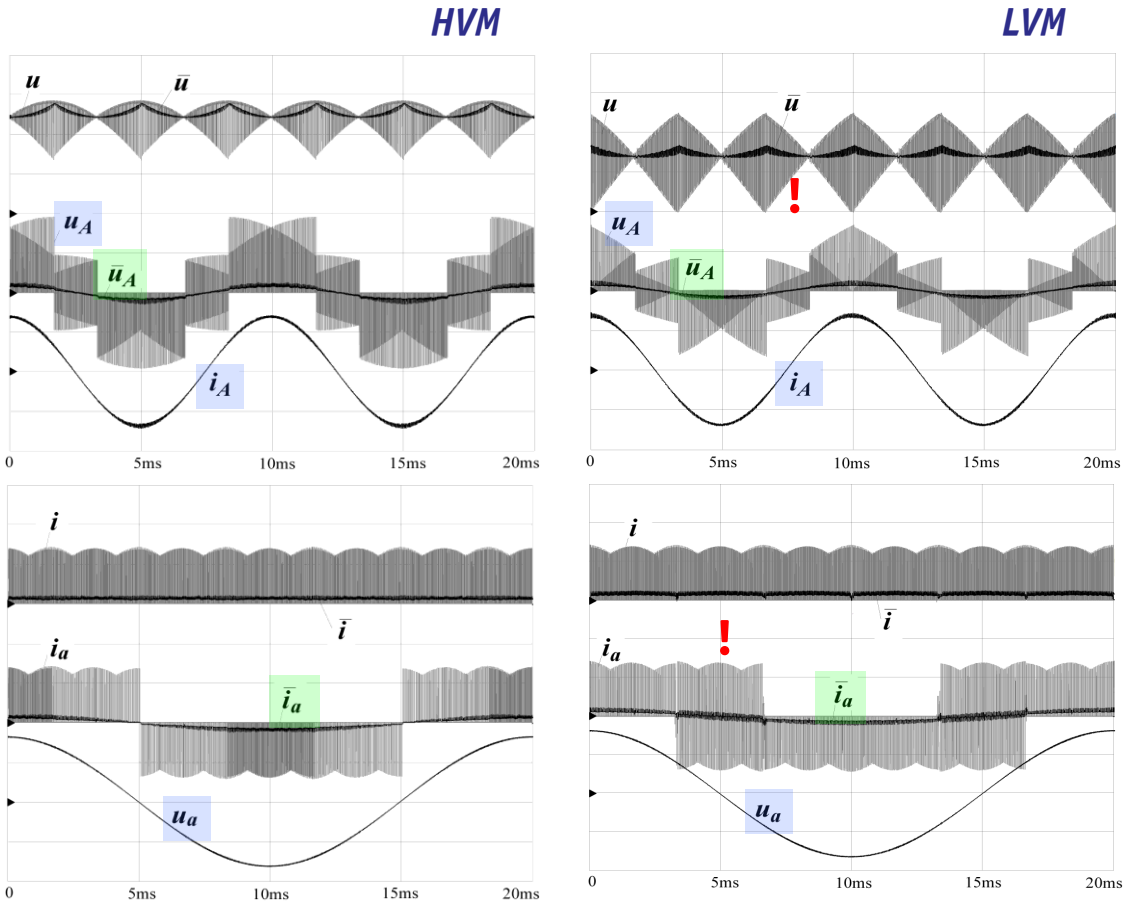
$$\hat{U}_2 = 0 \ldots \frac{1}{2} \cdot \hat{U}_1$$



Alternative Modulation Schemes 2/2

- *HV vs. LV Output Modulation*
- *Voltage & Current Time Behavior*

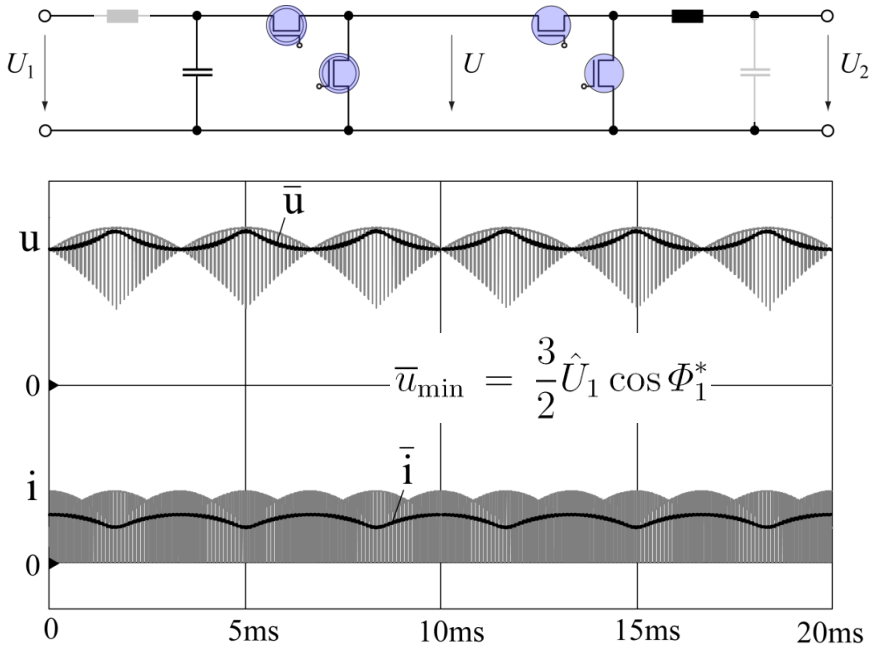


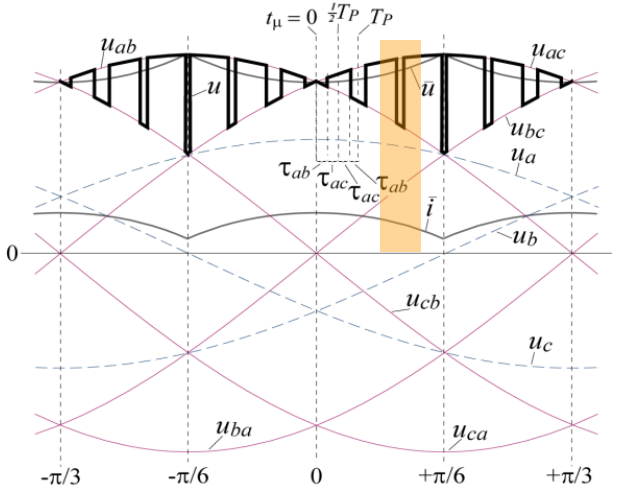


IMC Output Voltage Limit

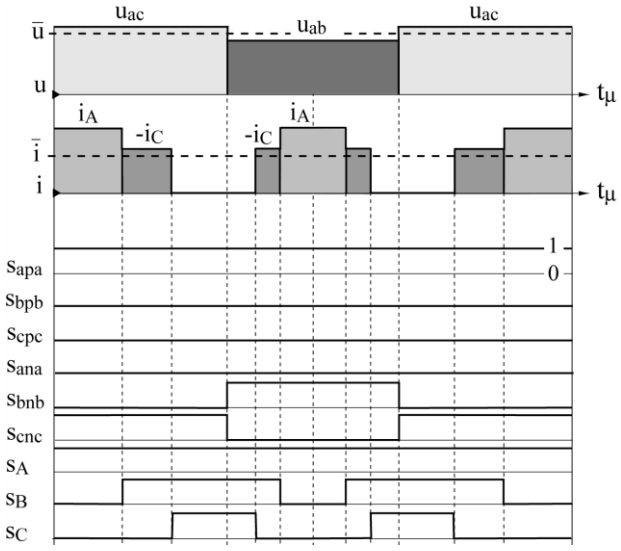
- *IMC — Cascaded Buck-Type Structure*
- *Input-Stage Output Voltage Reduces with cos Φ_1*
- *Analogous to Thyristor AC/DC Converter*

$$\hat{U}^*_{2,\max} \leq \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \cos \Phi^*_1 \quad !$$





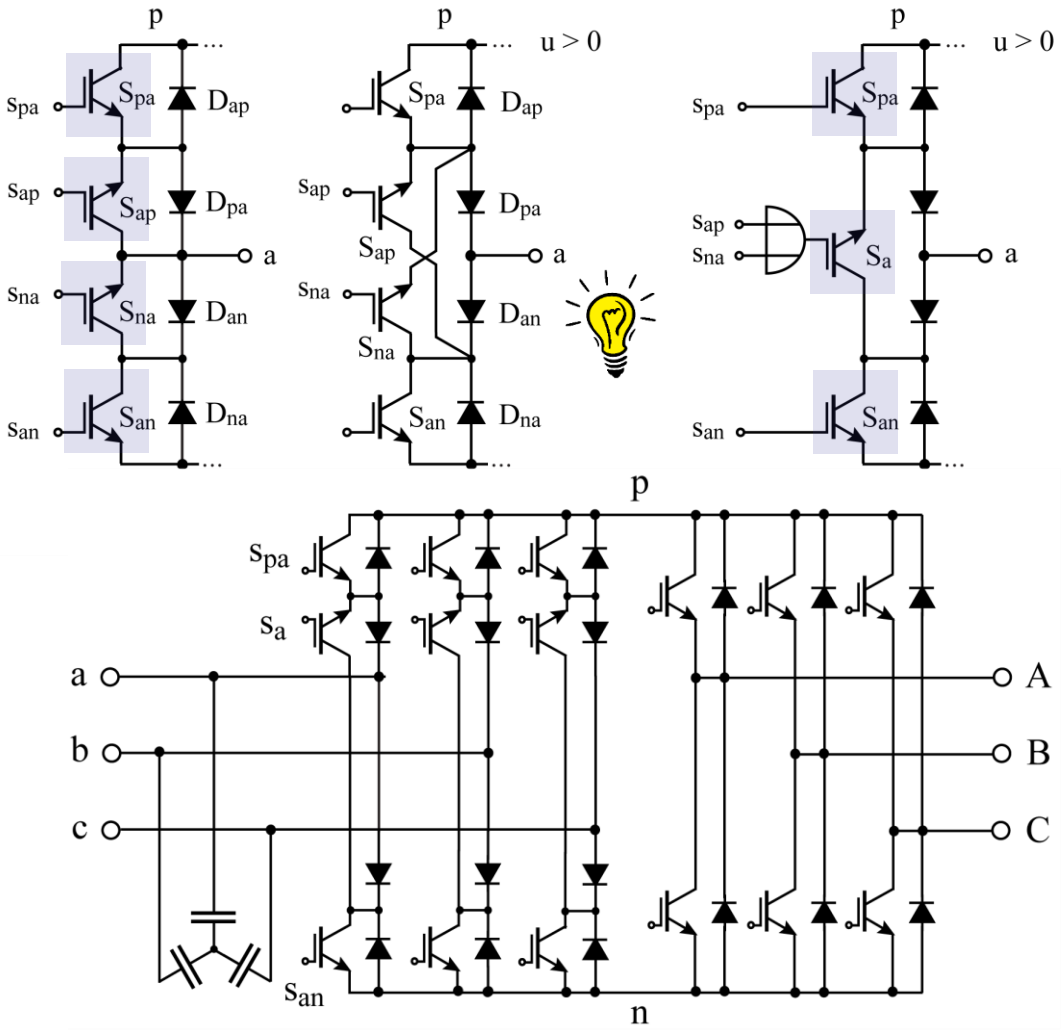
120° of Mains Period



DC-Link Voltage & Current

PWM Pattern

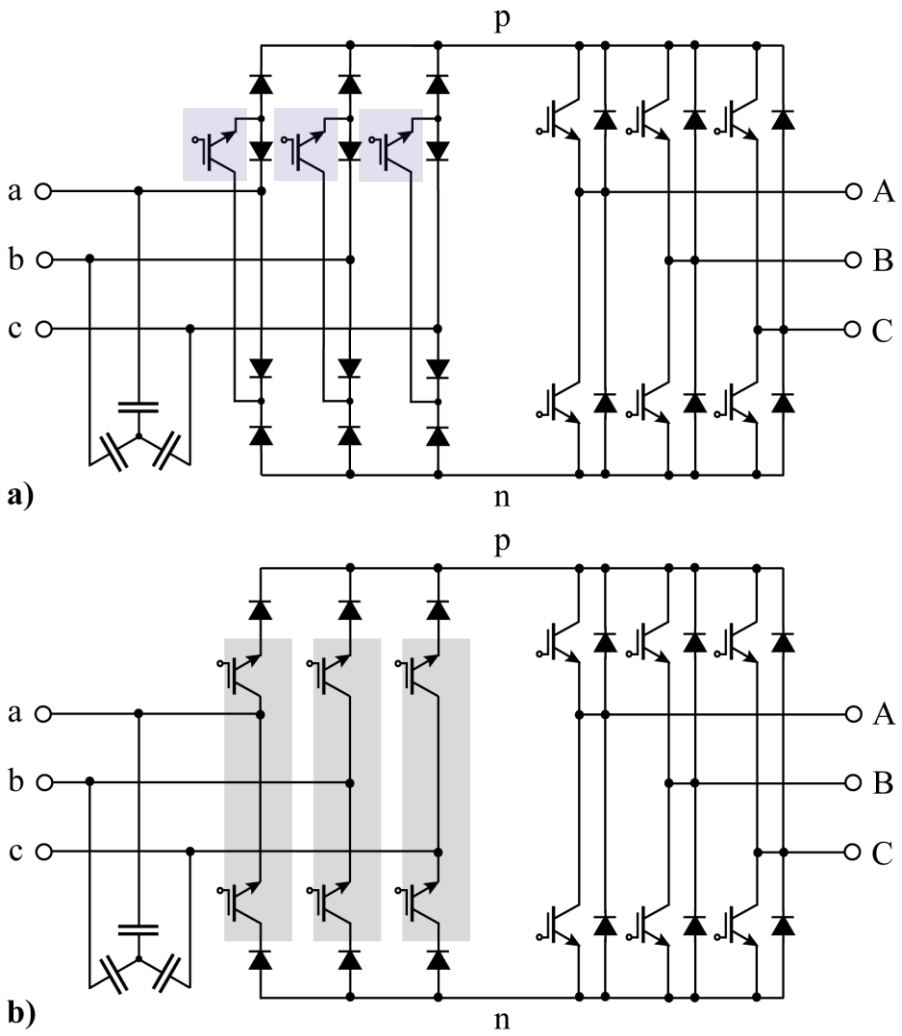
Sparse Matrix Converter



ETH Zurich

- *15 Transistors*
- *18 Diodes*

Ultra Sparse Matrix Converter

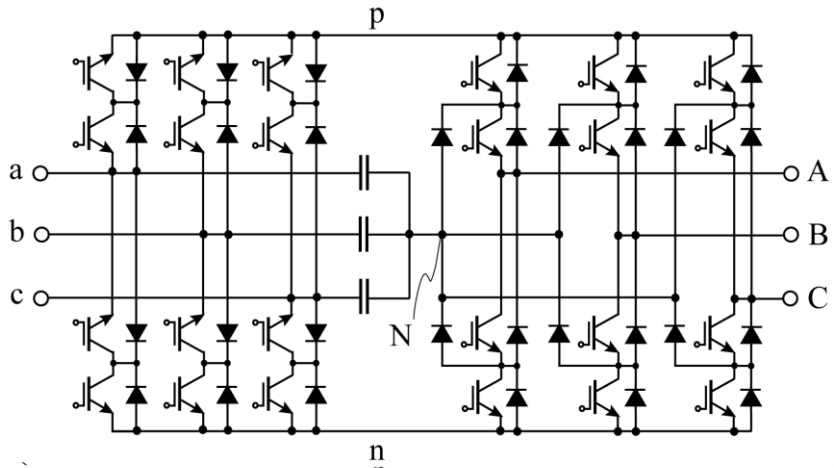


ETH Zurich
T. Lipo [13, 20]

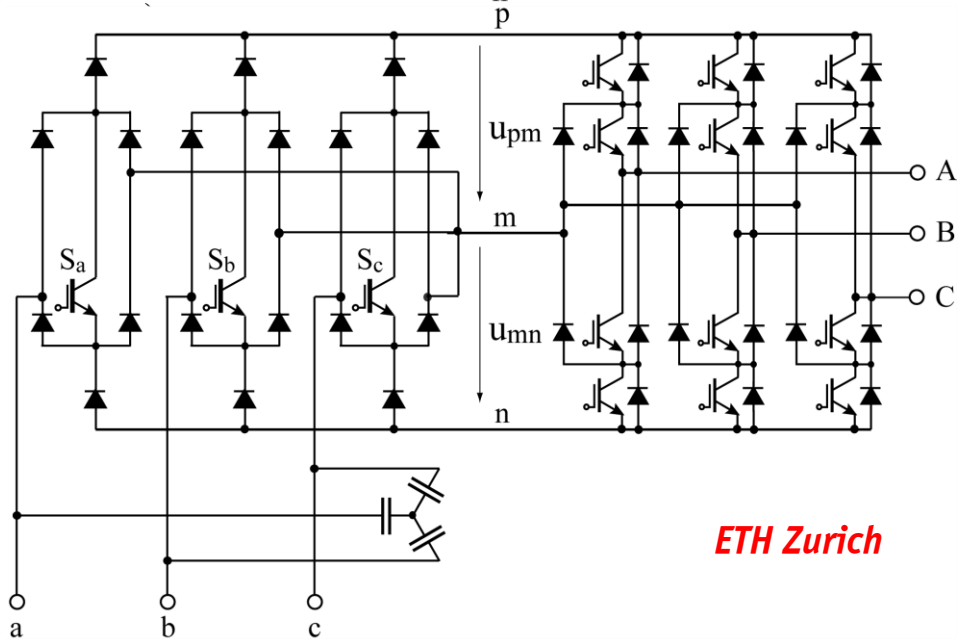
- *9 Transistors*
- *18 Diodes*

Three-Level Matrix Converter 1/2

- *Bidirectional Converter*

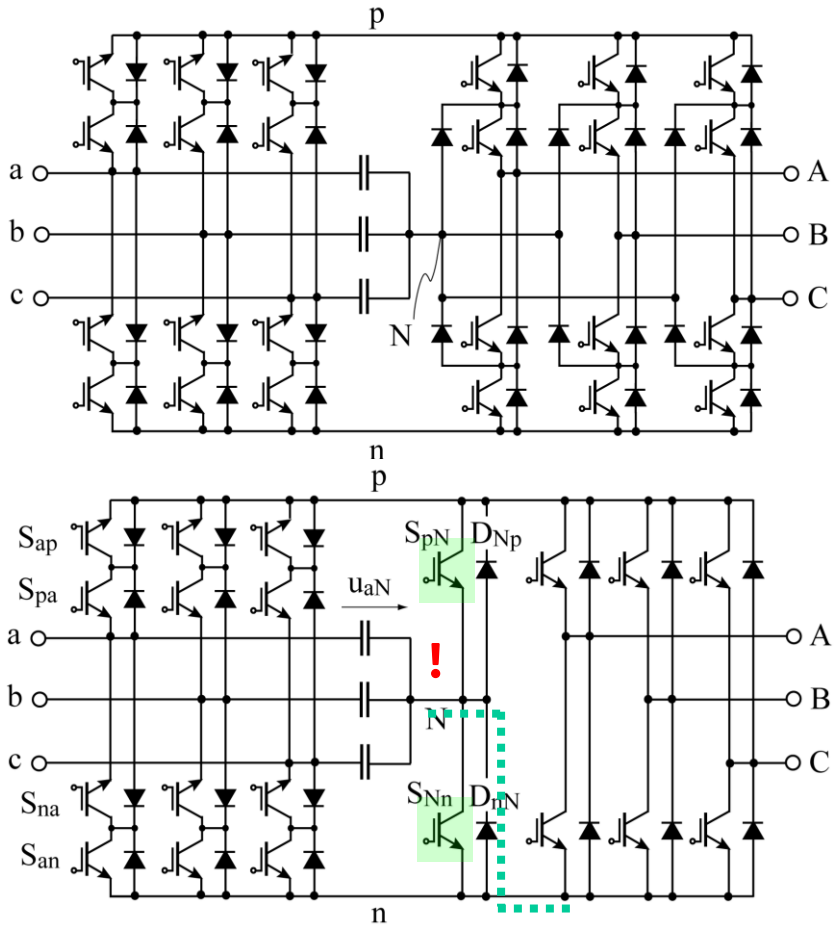


- *Unidirectional Converter*



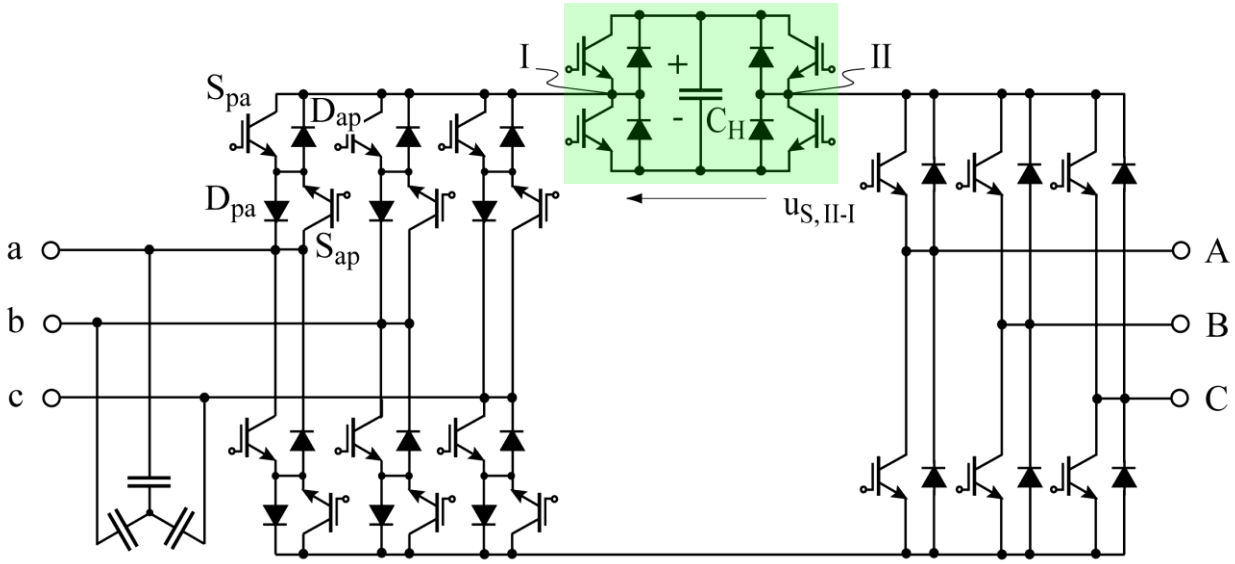
ETH Zurich

Three-Level Matrix Converter 1/2



Ch. Klumpner

Hybrid IMC

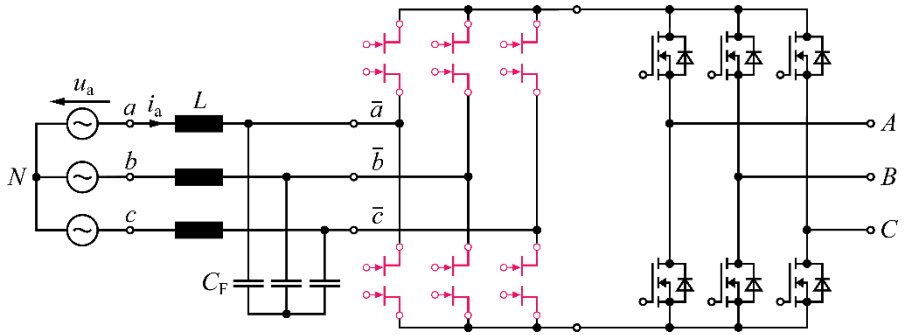


Ch. Klumpner

3-Φ AC/AC *Matrix* Converter Comparison

■ *Indirect Matrix Converter (IMC)*

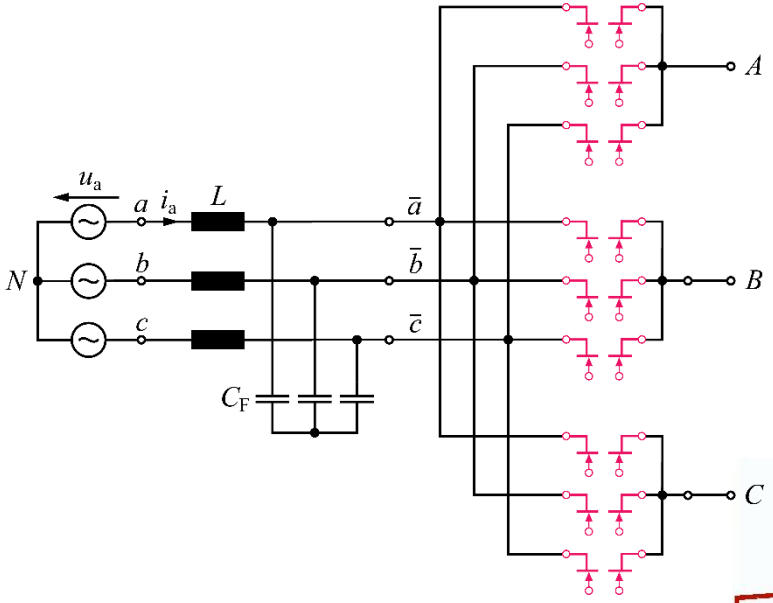
- *GaN M-BDS AC/DC Front-End*
- *ZCS Commutation of AC/DC Stage @ i_{DC}=0*
- *No 4-Step Commutation*



- *Higher # of Switches Compared to DMC*
- *Lower Cond. Losses @ Low Output Voltage*
- *Thermally Critical @ f_{out} → 0*

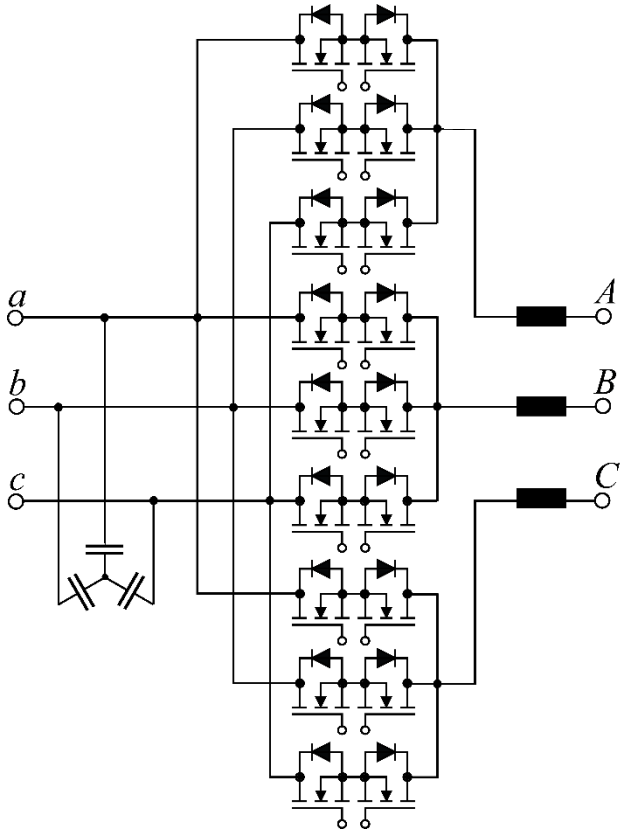
■ *Direct Matrix Converter (CMC)*

- *4-Step Commutation*
- *Exclusive Use of GaN M-BDSs*

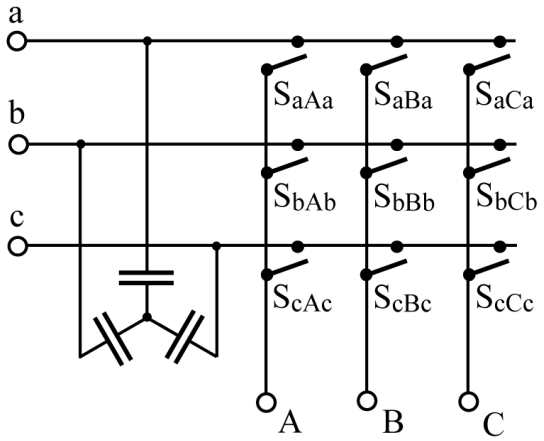


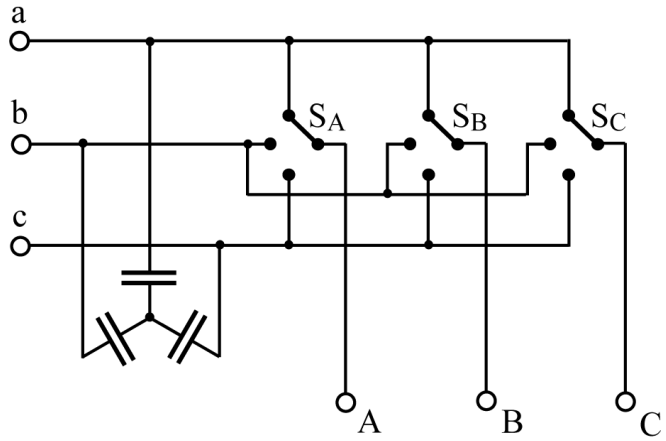
- *Thermally Critical @ $f_{out} \approx f_{in}$*

Direct Matrix Converter (DMC)



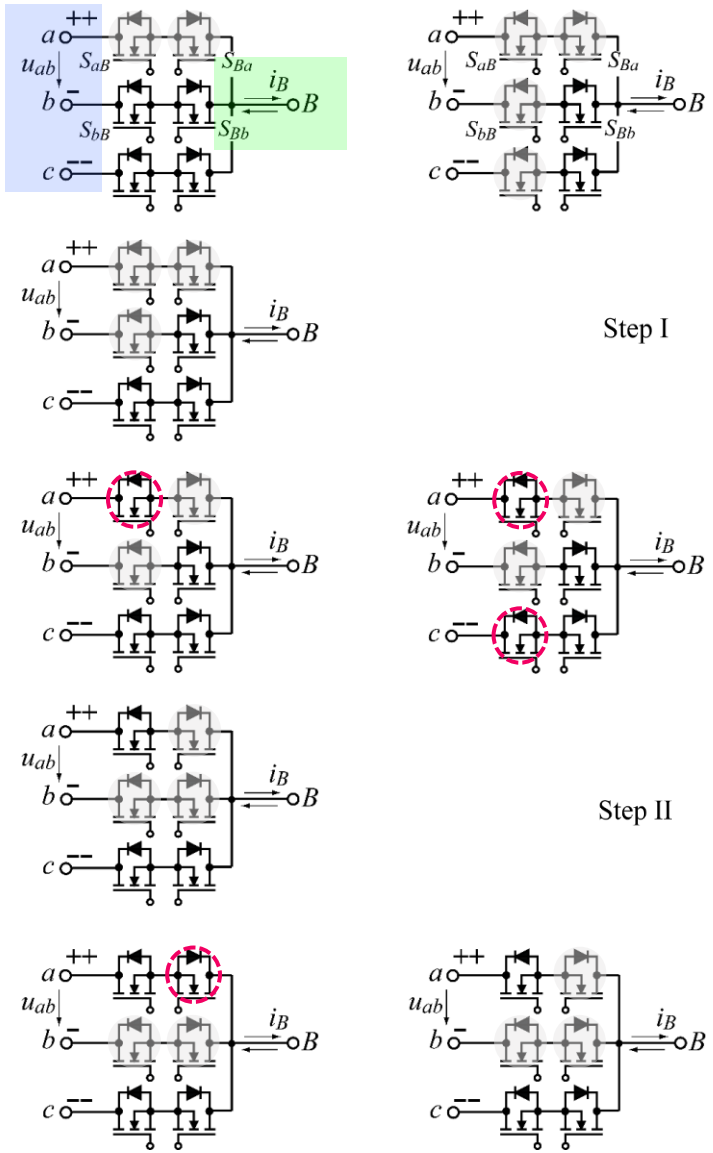
- *Direct AC/AC Conversion → 4-Quadrant (AC) Switches*
- *Quasi Three-Level Output Characteristic*





- *Multi-Step Commutation (!)*
- *Prevent Mains Short Circuit & Interruption of Load Current*

DMC Multi-Step Commutation

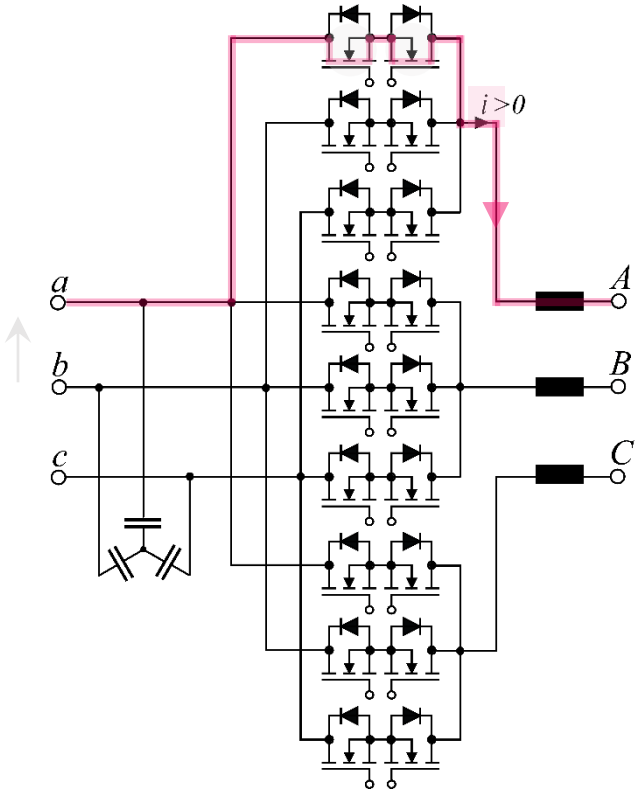


Example ***u-Dependent Commutation aB → bB @ $u_{ab} > 0$***

- ***Four-Step Commutation***
- ***Two-Step Commutation***

4-Step Commutation of DMC

- *Example* *i-Dependent Commutation*
  aA → bA @ i > 0



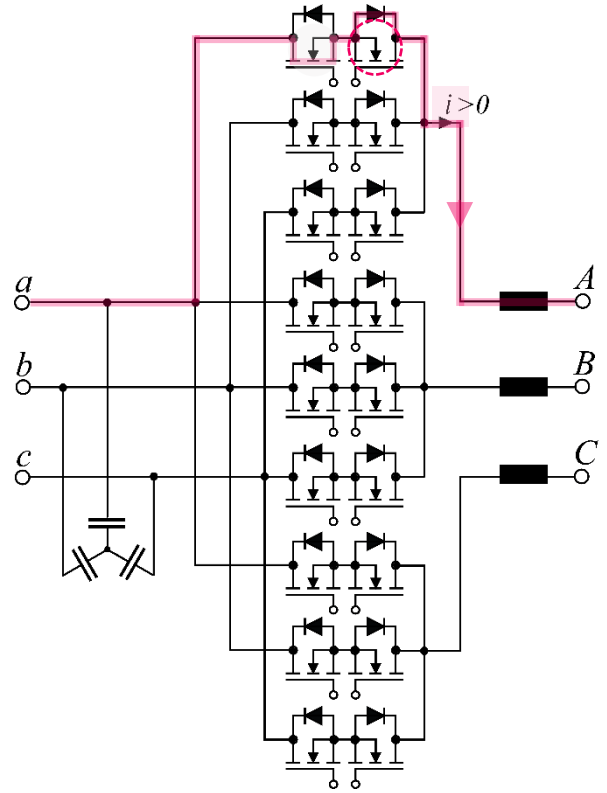
- *No Mains Short Circuit*
- *No Load Current Interruption*

Assumption $u_{ab} < 0$

4-Step Commutation of DMC 1/4

- *Example* *i-Dependent Commutation*
  aA → bA @ i > 0

1st Step: **Off**



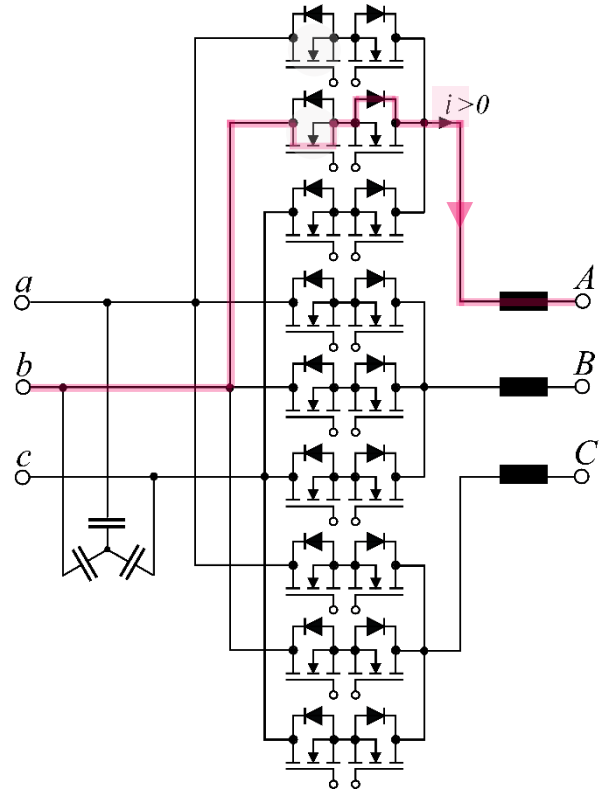
- *No Mains Short Circuit*
- *No Load Current Interruption*

Assumption $u_{ab} < 0$

4-Step Commutation of DMC 2/4

- *Example* *i-Dependent Commutation*
  aA → bA @ i > 0

1st Step: Off
2nd Step: On



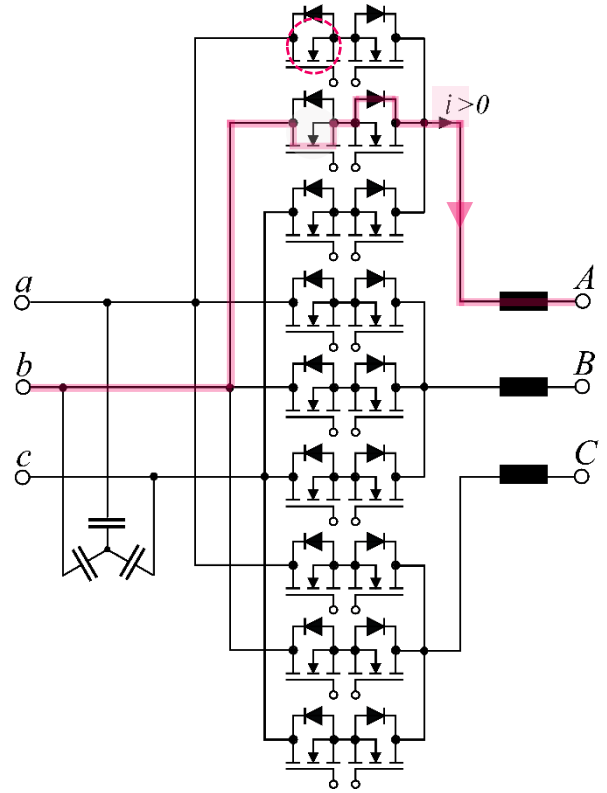
- *No Mains Short Circuit*
- *No Load Current Interruption*

Assumption $u_{ab} < 0$

4-Step Commutation of DMC 3/4

- *Example* *i-Dependent Commutation*
  aA → bA @ i > 0

1st Step: Off
2nd Step: On
3rd Step: Off



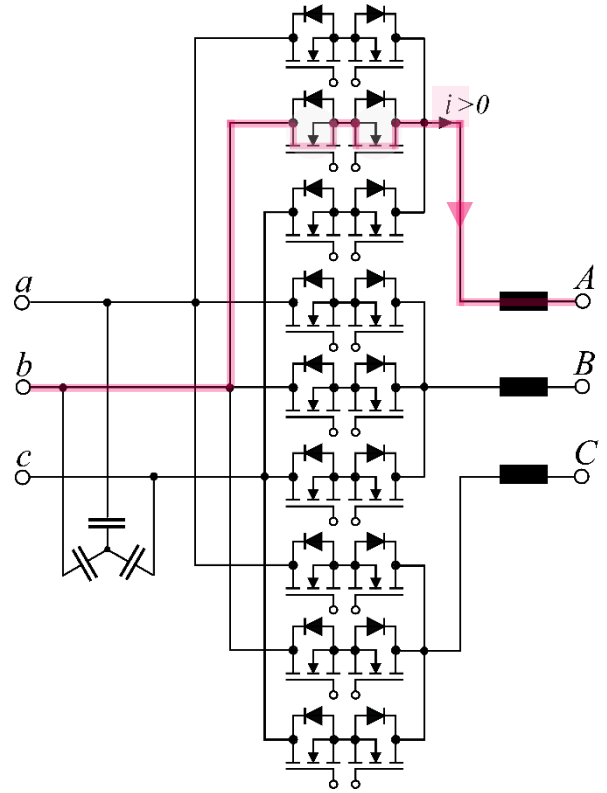
- *No Mains Short Circuit*
- *No Load Current Interruption*

Assumption $u_{ab} < 0$

4-Step Commutation of DMC 4/4

- *Example* *i-Dependent Commutation*
  aA → bA @ i > 0

1st Step: Off
2nd Step: On
3rd Step: Off
4th Step: On

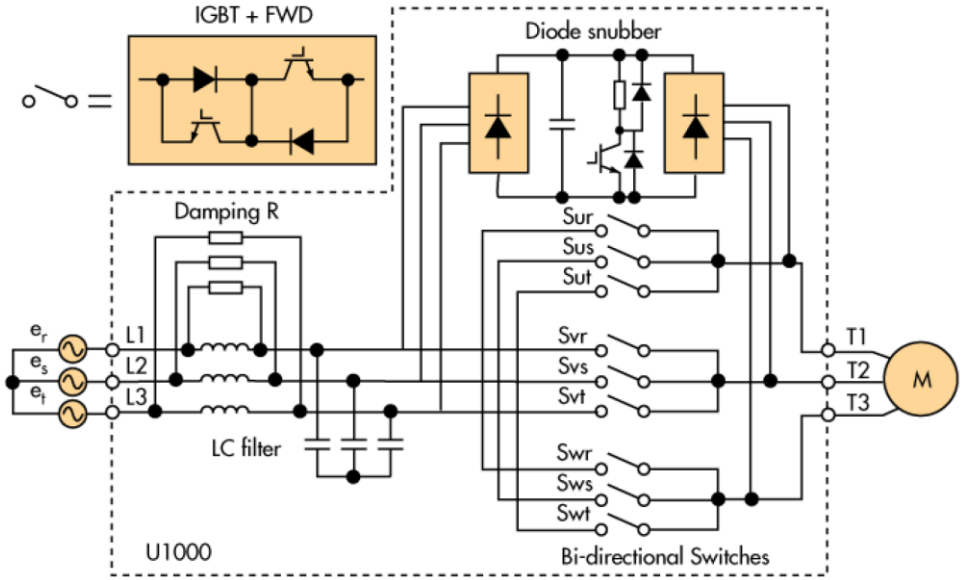


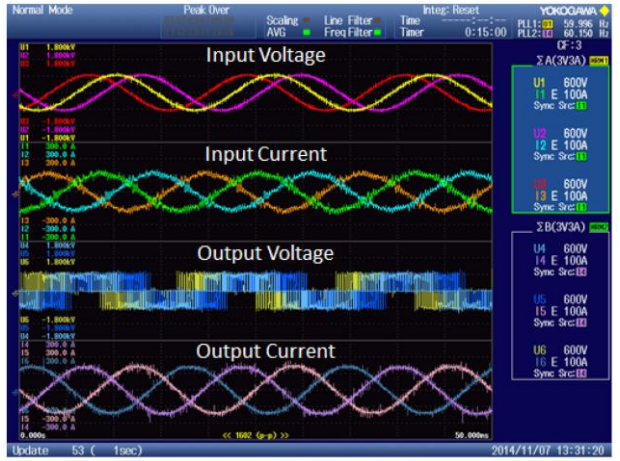
- *No Mains Short Circuit*
- *No Load Current Interruption*

Assumption $u_{ab} < 0$

Industry Application of 3-Φ Matrix Converter

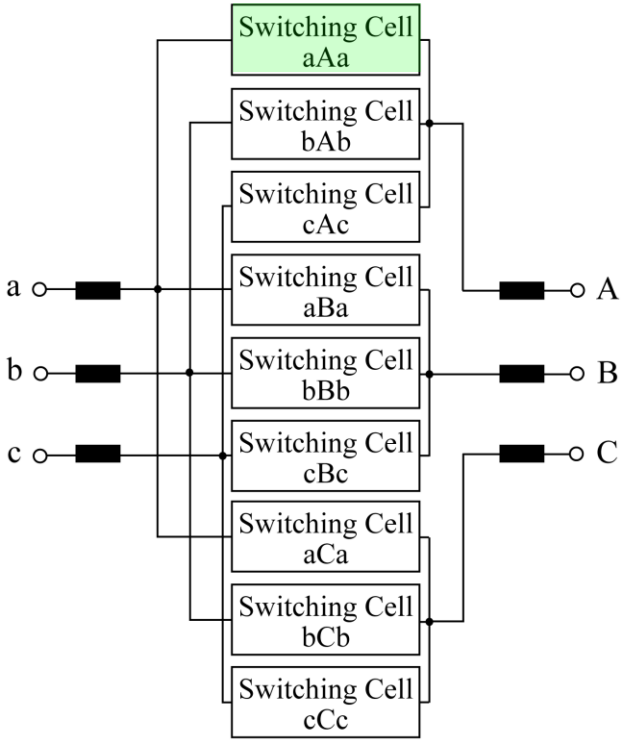
- *Fully Regenerative → e.g. Downhill Conveyor etc.*
- *Higher Power Density Compared to Voltage DC-Link System / No Front-End Boost Inductors*
- *Quasi Three-Level Output Characteristic*
- *No-Switching / Eco Operation for $f_2 = f_{Mains}$*
- *Close to Unity Power Factor*

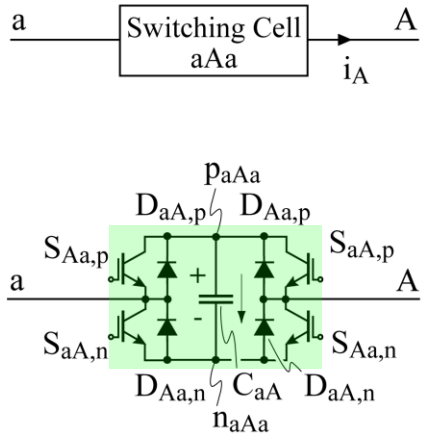




- *Challenging Overvoltage Protection*
- *Limited Output Voltage Range (!)*

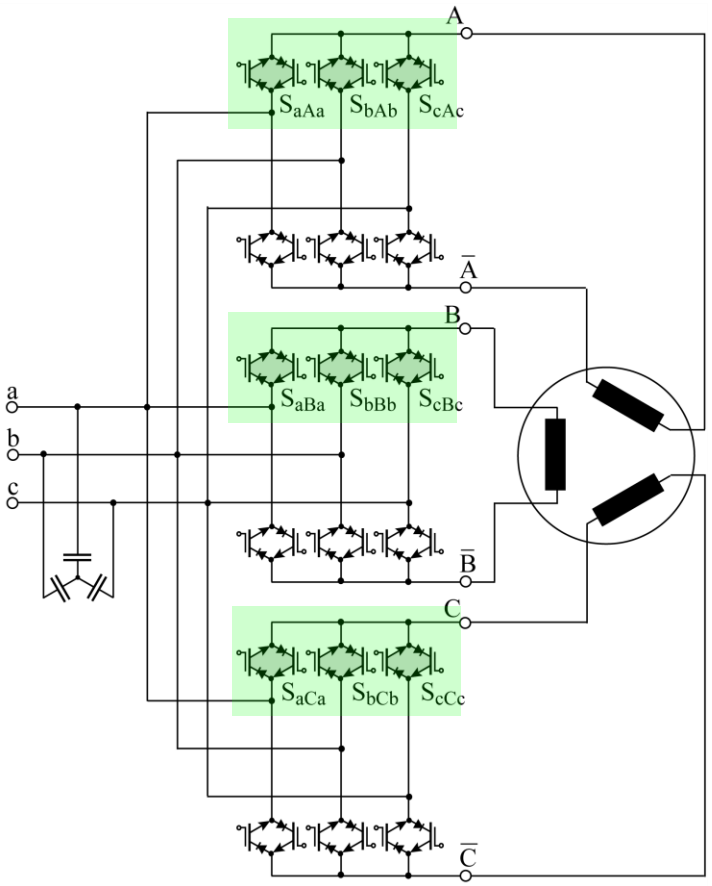
Hybrid CMC

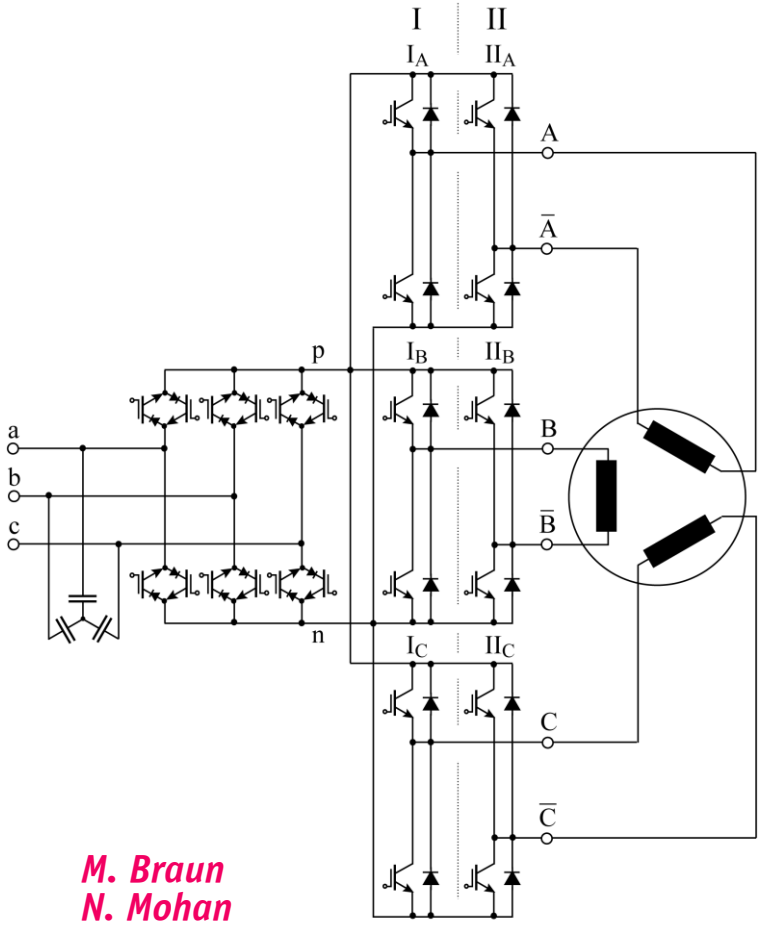




B. Erickson

Full-Bridge CMC / IMC

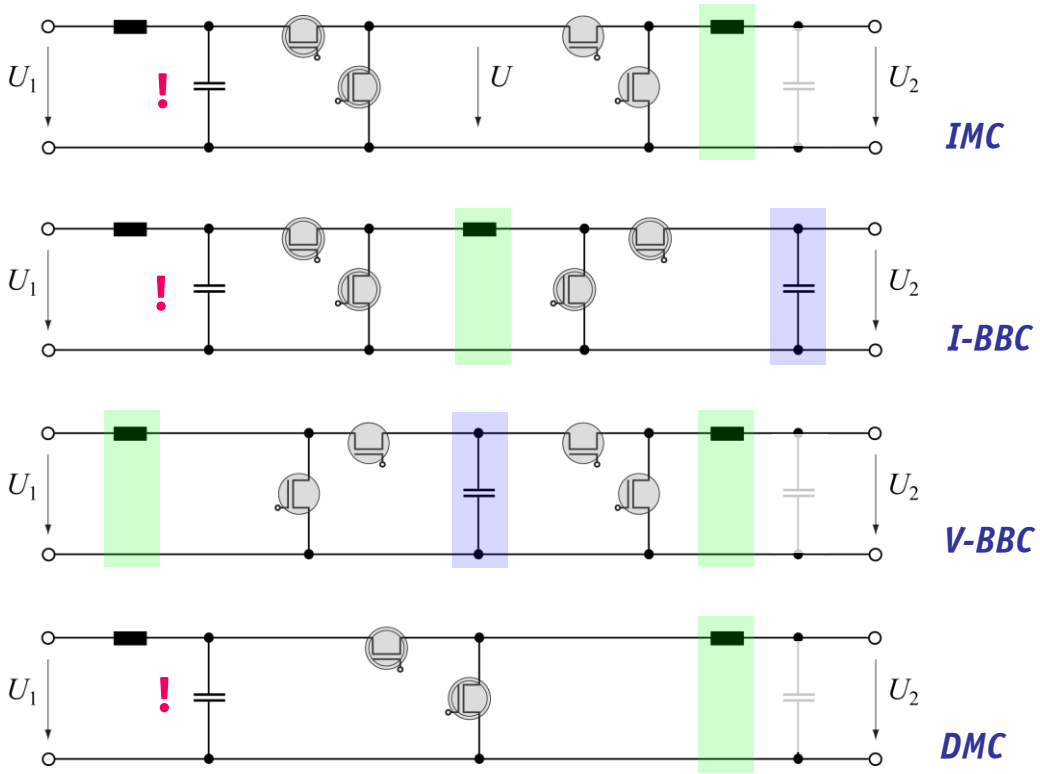




M. Braun
N. Mohan

Control Properties of 3-Φ AC-AC Converters

! *Uncontrolled Input Filter*

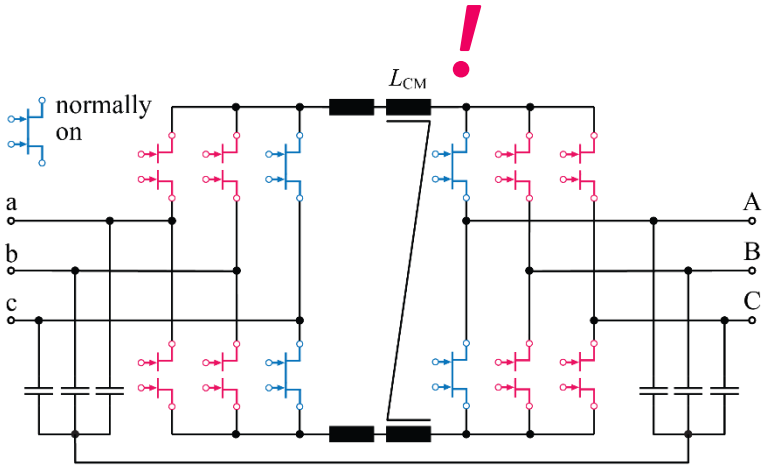


- *DC-DC Equivalent Circuits*

3-Φ Current DC-Link vs. Matrix AC/AC Converter

Current DC-Link Topology

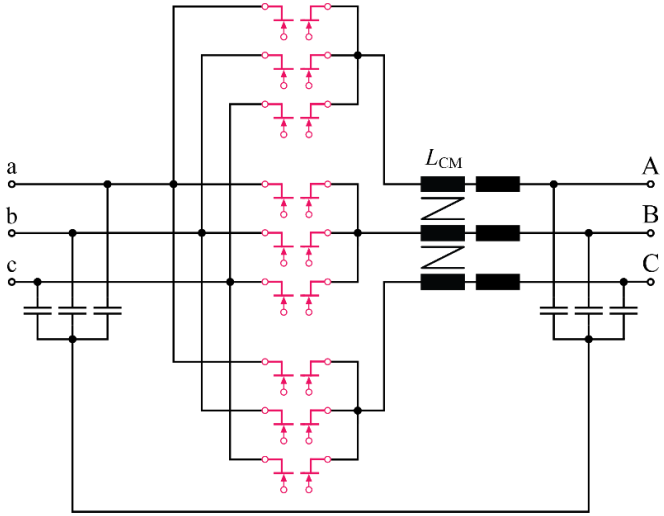
- Application of M-BDSs | 12 Switches
- 4-Step Commutation
- Buck-Boost Functionality
- Low Filter Volume



- Challenging Overvoltage Protection

Direct Matrix Converter

- Application of M-BDSs | 9 Switches
- 4-Step Commutation
- Complex Space Vector Modulation
- Limited to Buck-Operation (!)



- Challenging Overvoltage Protection

Outlook

Summary

- *Future Need for „SWISS Knife“-Type Inverter Systems*

— *Wide Input / Output Voltage Range*
— *Continuous / Sinusoidal Output Voltage*
— *Electromagnetically „Quiet“ - No Shielded Cables*
— *“Plug & Play“ / Non-Expert Installation*
— *SMART Motors / Cognitive VSDs*
— *On-Line Monitoring / Industry 4.0*

Source: UK Outdoor Store

- *Enabling Technologies*

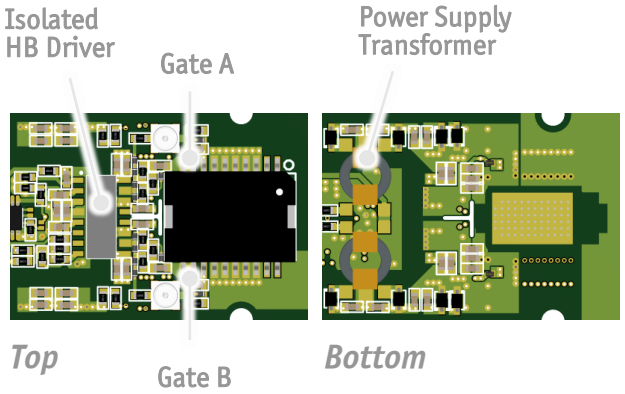
— *SiC / GaN*
— *Advanced (Multi-Level) Topologies*
— *“Synergetic” Control*
— *Monolithic Bidirectional GaN*
— *Integration of Switches / Gate Drives / Sensing / Monitoring*
— *Adv. Modeling / Simulation / Optimization*
— *Machine Learning / AI*

- *System Level → Distributed DC Bus Systems, Integration of Storage, etc.*

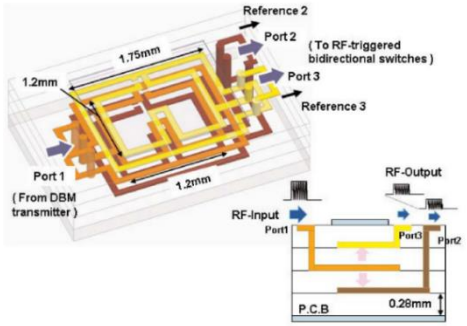
Monolithic 3D-Integration

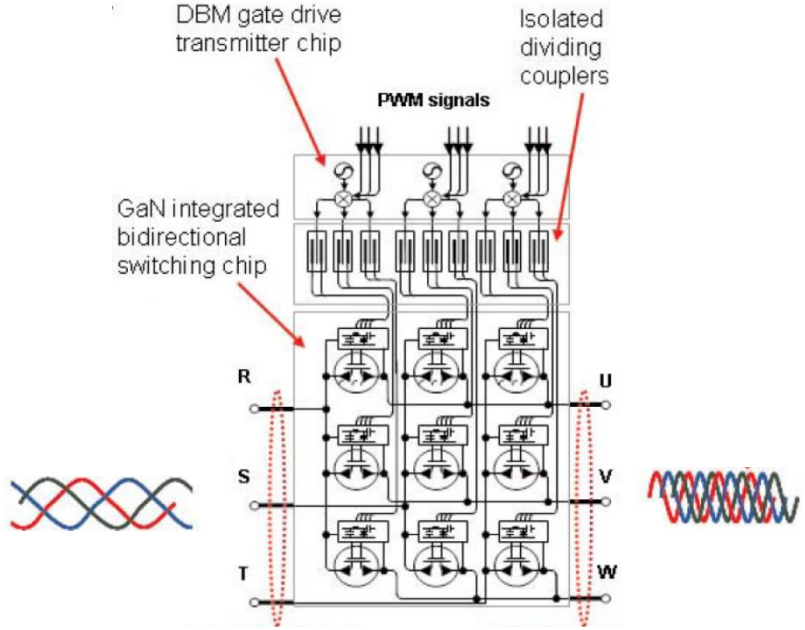
Source: Panasonic ISSCC 2014

- *M-BDS GaN 3x3 Matrix Converter with Drive-By-Microwave (DBM) Technology*
  - *9 Dual-Gate GaN AC-Switches / 4-Step Commutation*
  - *DBM Gate Drive Transmitter Chip & Isolating Couplers*
  - *Ultra Compact → 25 x 18 mm² (600 V, 10 A – 5 kW Motor)*



5.0GHz Isolated (5 kV_{DC}) Dividing Coupler

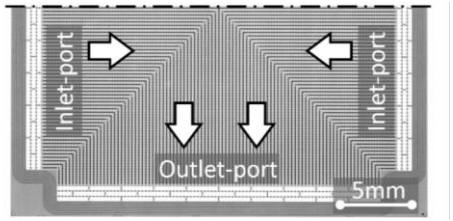


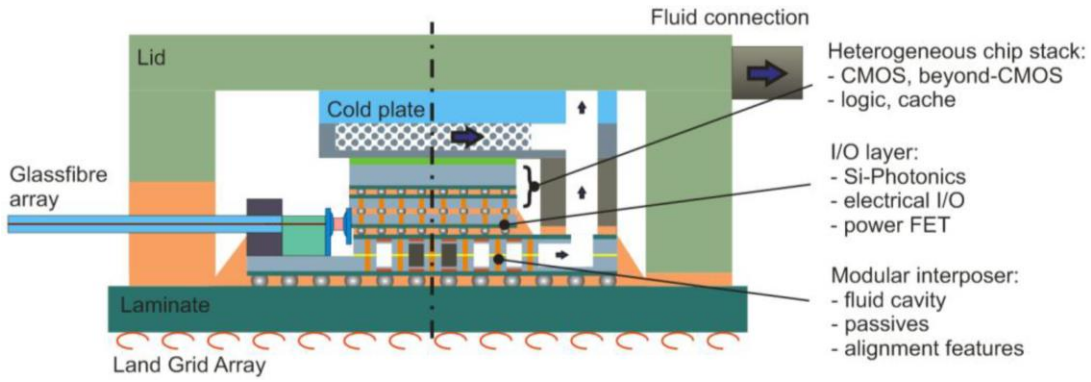


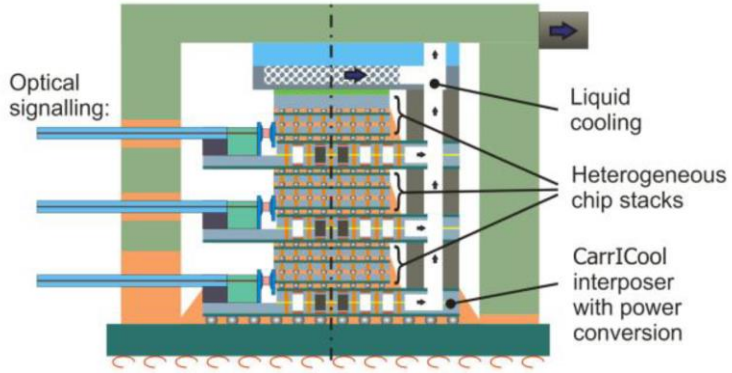
- *Massive Space Saving Compared to Discrete Realization (!)*

Remark Future uP Chip-Stack Packaging

- *Slowing Transistor Node Scaling → Vertical & Heterogeneous Integr. of ICs for Performance Gains*
- *Extreme 3D-Integrated Cube-Sized Compute Nodes*
- *Dual Side & Interlayer Microchannel Cooling*



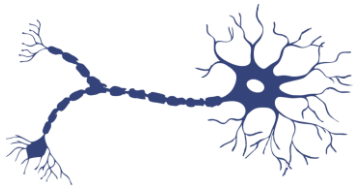




- *Interposer Supporting Optical Signaling / Volumetric Heat Removal / Power Conversion*

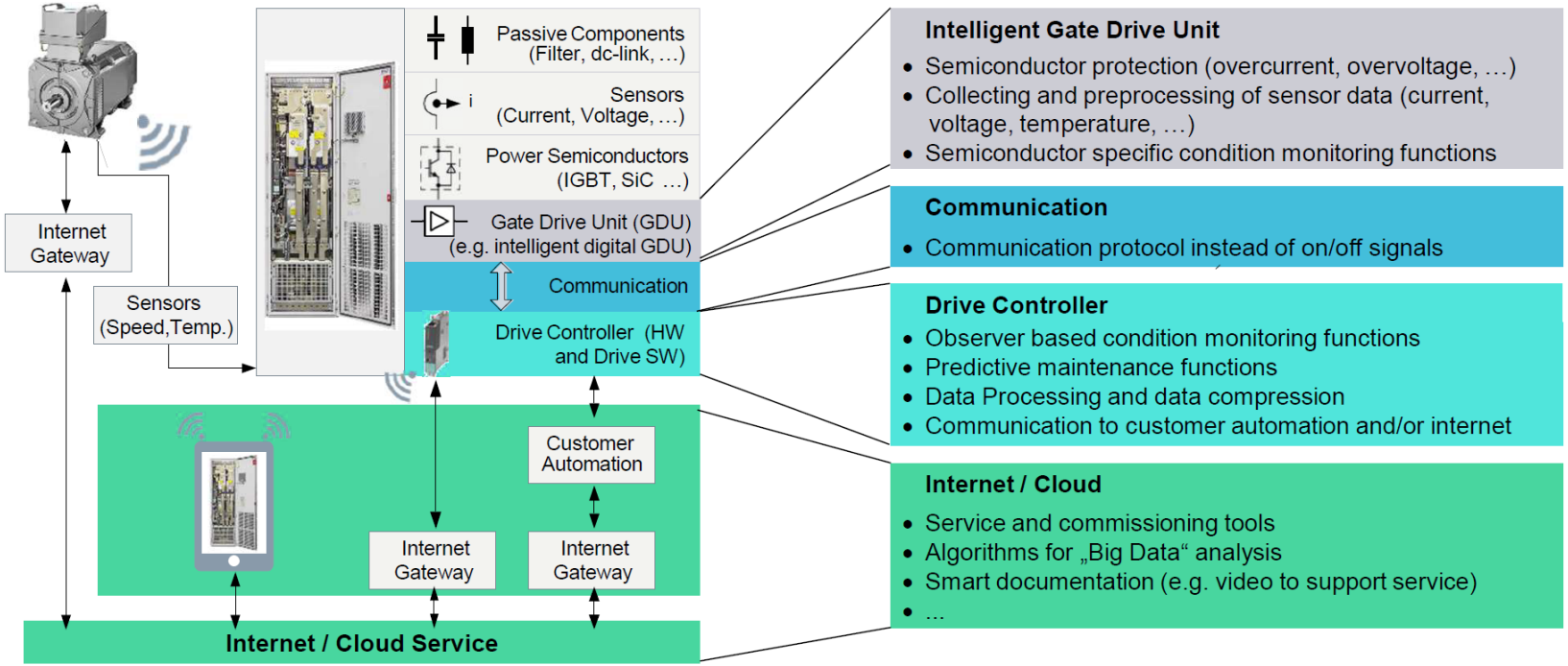
CarrICool
EU FP7 Project

Smart Converter Concept



- *Utilize High Computing Power & Network Effects in the Cloud → "Cognitive" Power Electronics*

Source: Dr. R. Sommer
SIEMENS



- *Sensing & Computing on Component Level | Converter Level | System Level | Application Level*

Thank you!

Acknowledgement

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M. Haider
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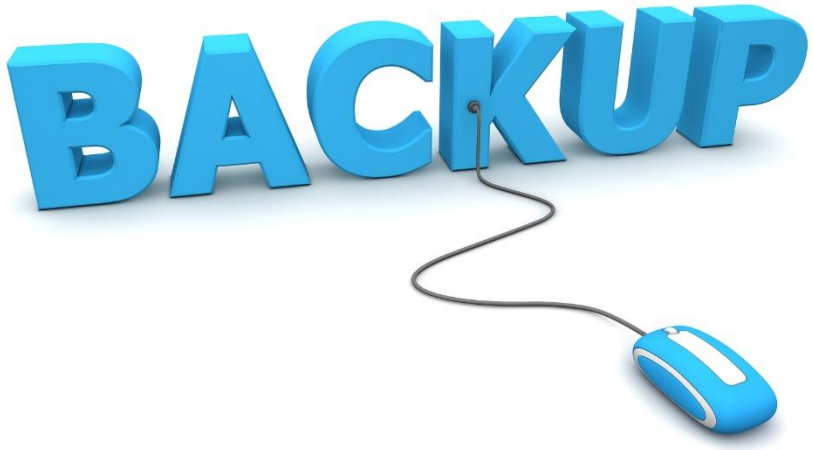
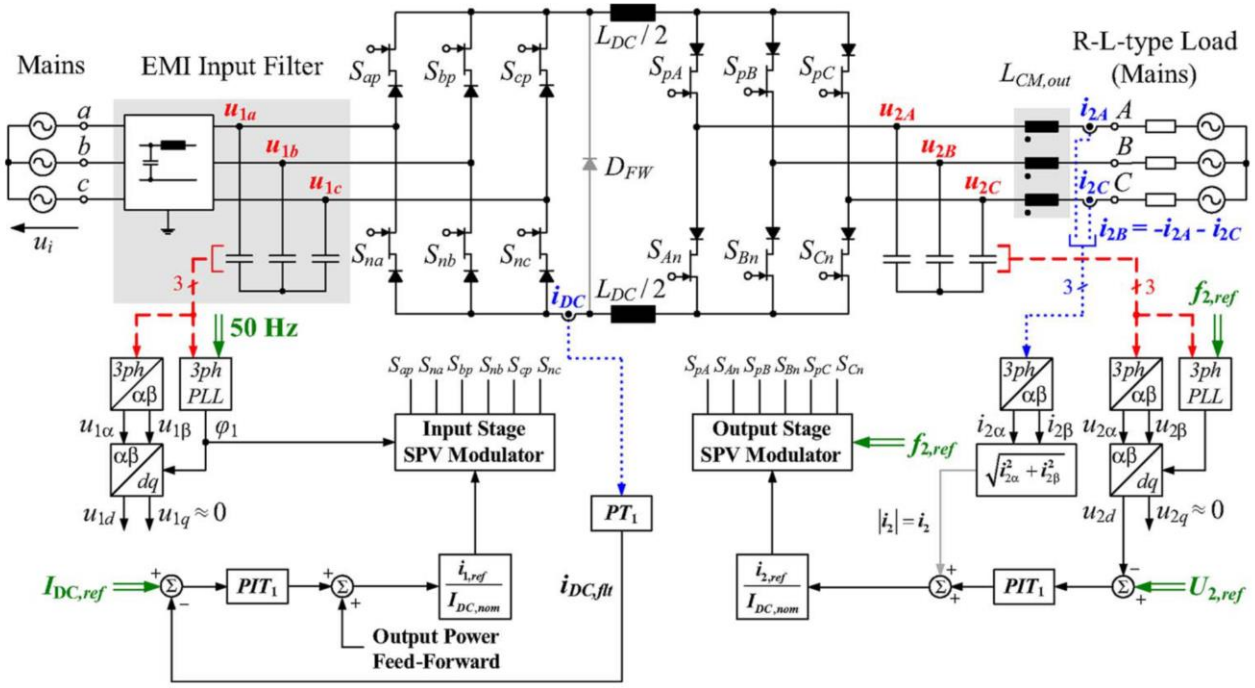
N. Nain
P. Niklaus
S. Weihe
D. Zhang


BACKUP

200kHz SiC Current DC-Link AC/AC Converter (1)

- *Normally-On TO-220 1200V/6A SiC J-FETs — Built in 2008 (!)*
- *1200V/10A SiC Schottky Series Diodes*
- *X7R Ceramic Filter Capacitors*

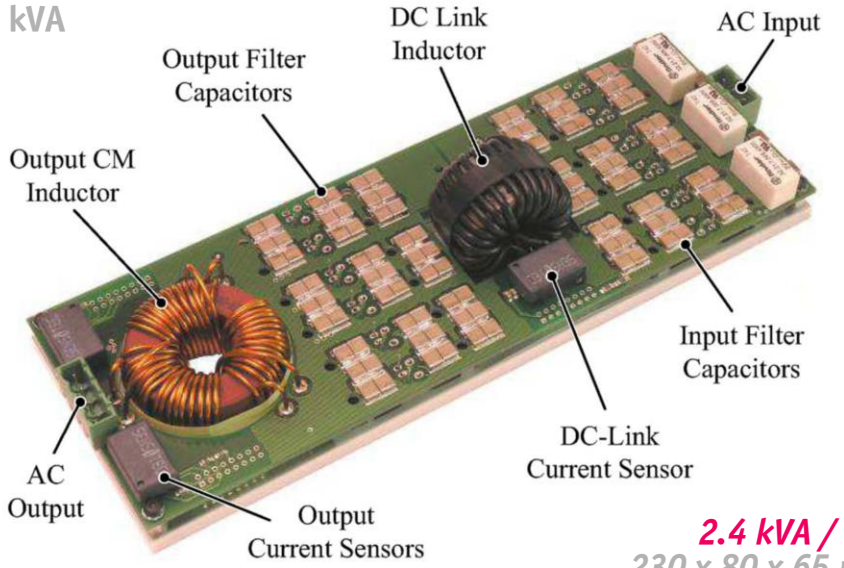


- *Normally-On J-FETs — Natural Free-Wheeling Current Path for Gate Driver Failure*

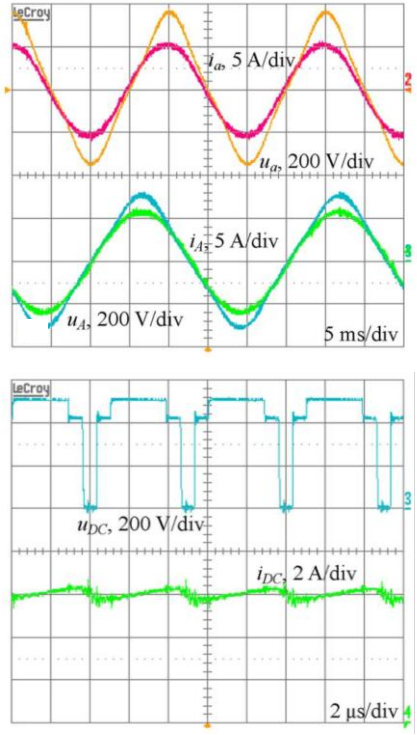
200kHz SiC Current DC-Link AC/AC Converter (2)

- *Normally-On TO-220 1200V/6A SiC J-FETs — Built in 2008 (!)*
- *1200V/10A SiC Schottky Series Diodes*
- *X7R Ceramic Filter Capacitors*

Input	$400V_{rms}$ Line-to-Line
Output	0...300Hz
Rated Power	2.5 kVA



2.4 kVA / dm³
230 x 80 x 65 mm³

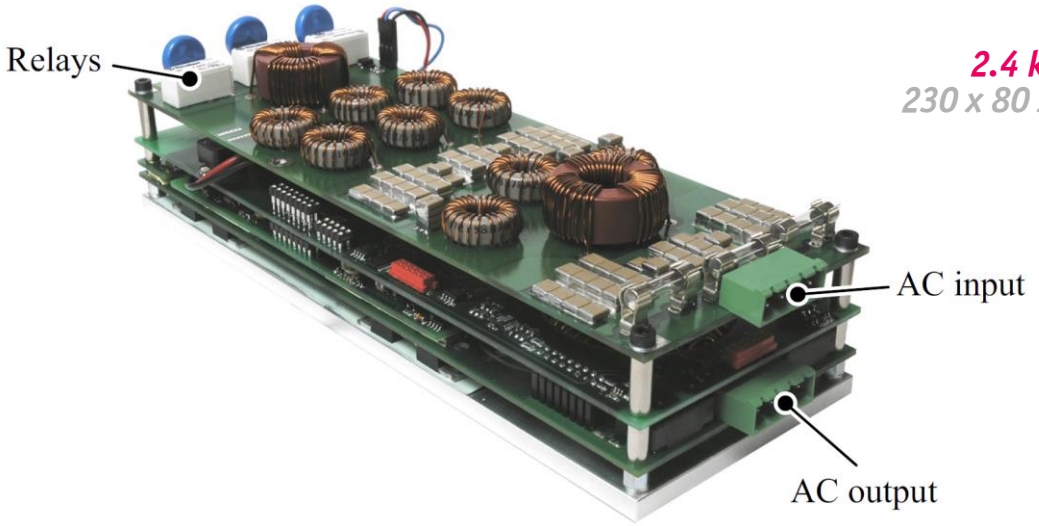


- *Low Volume DC-Link Inductor (320uH)*

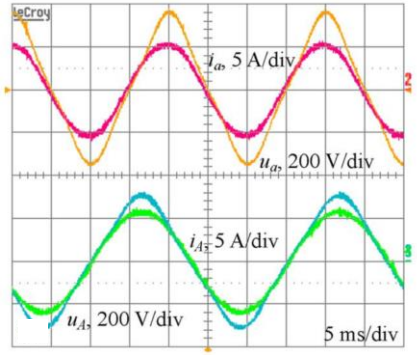
200kHz SiC Current DC-Link AC/AC Converter (3)

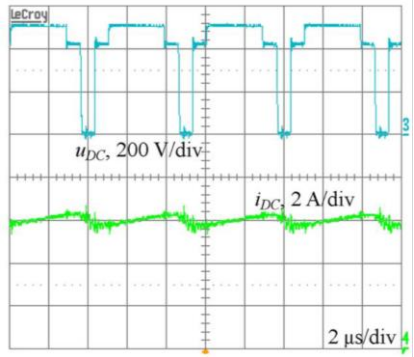
- *7kHz DC-Link Current Control Bandwidth*
- *PCB-Stack Construction — Power | Gate-Drive | Control Board*
- *Coldplate Cooling*

Input	400V_{rms} Line-to-Line
Output	0...300Hz
Rated Power	2.5 kVA



2.4 kVA / dm³
230 x 80 x 65 mm³



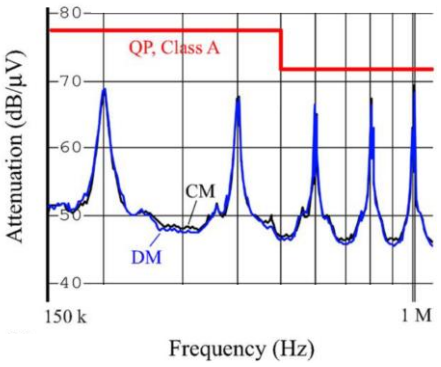


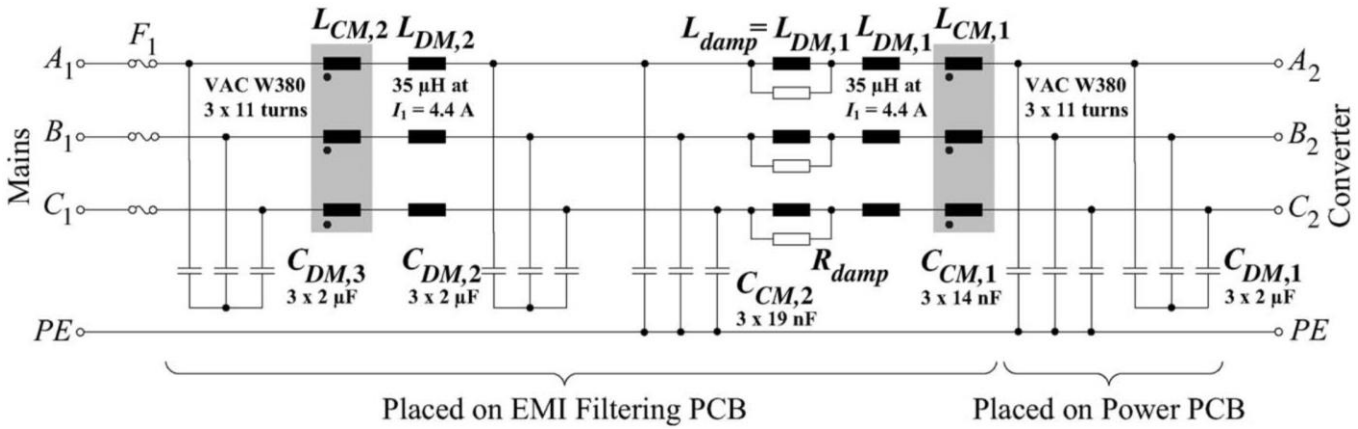
- *Low Volume DC-Link Inductor (320uH)*

200kHz SiC Current DC-Link AC/AC Converter (4)

- *7kHz DC-Link Current Control Bandwidth*
- *PCB-Stack Construction — Power | Gate-Drive | Control Board*
- *Coldplate Cooling*

— **Conducted EMI | EMI Filter**





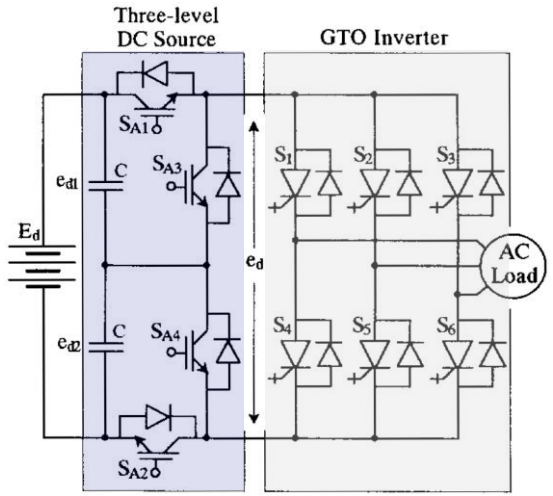
- *Low Volume Powder Core DC-Link Inductor (320uH)*

3-Level NPC Inverter / Sparse NPC Inverter

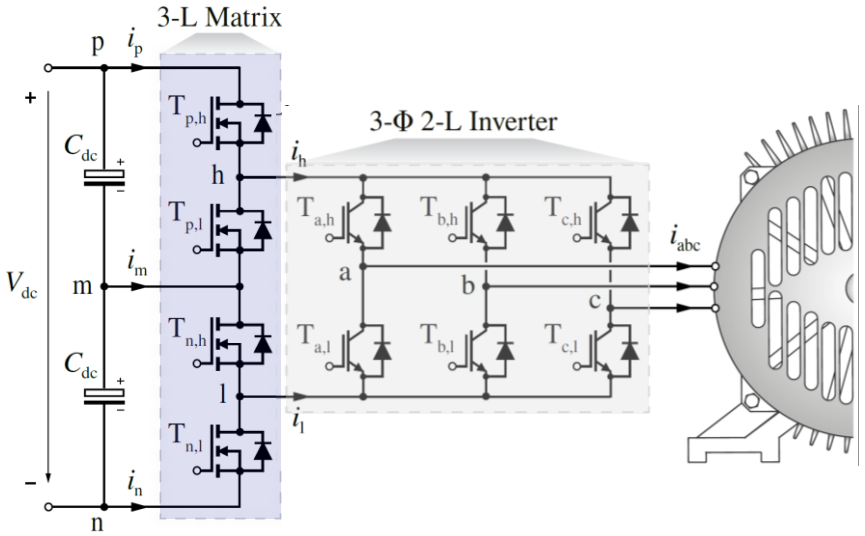
Sparse NPC 3-Level Inverter (1)

- *3-Level Neutral Point Clamped (3L-NPC) Topology Proposed in 1979 (Baker)*
- *Sparse NPC Converter (S-NPCC) → Reduced Total # of Switches*
- *Fast/Slow & Low/High Voltage Semiconductors ("Hybrid")*

- *Rojas (1993)*



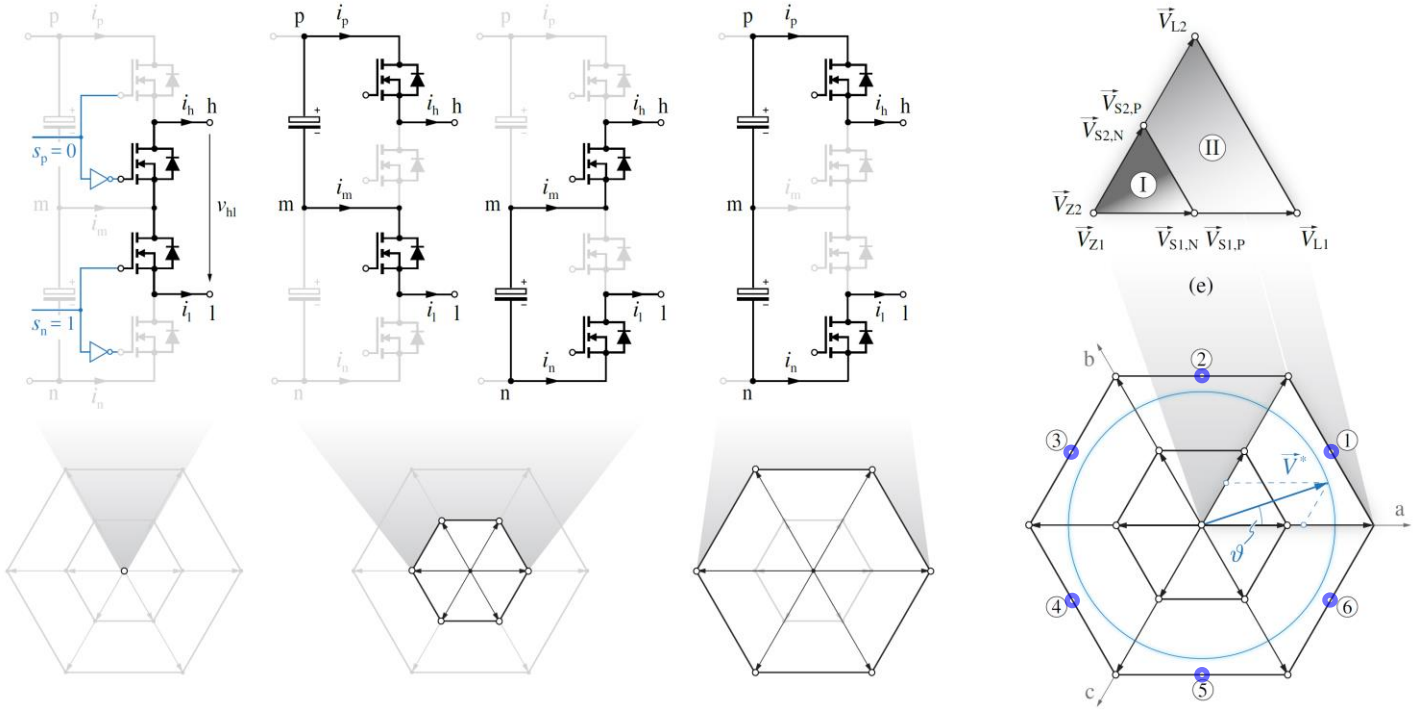
$+E, e_{d1}, e_{d2}, 0$



- *Realization of the S-NPCC Using 650V GaN HEMTs & 1200V Si IGBTs*

Sparse NPC 3-Level Inverter (2)

- *3-L Matrix Stage → "Voltage Pre-Conditioning" / 2-L Inverter Defines Voltage Direction*
- *Redundant Half Voltage States for DC Midpoint Balancing*



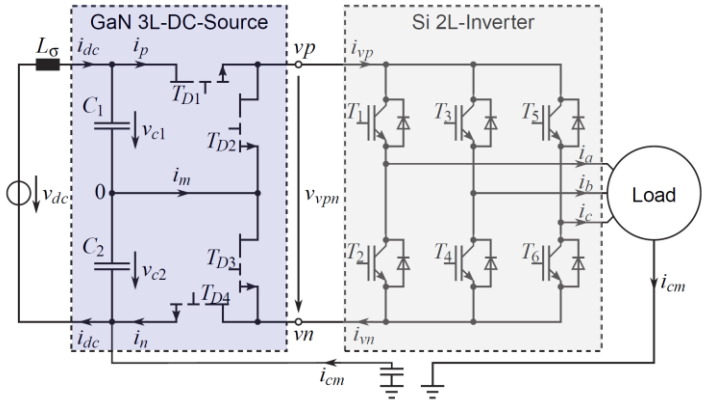
- *Missing Sw. States Compared to Full 3L-NPC → 7 Instead of 9 Phase Voltage Levels*
- *Diff. Sw. Schemes → E.g. Avoiding Commutation of 2L-Stage @ Full DC Voltage*

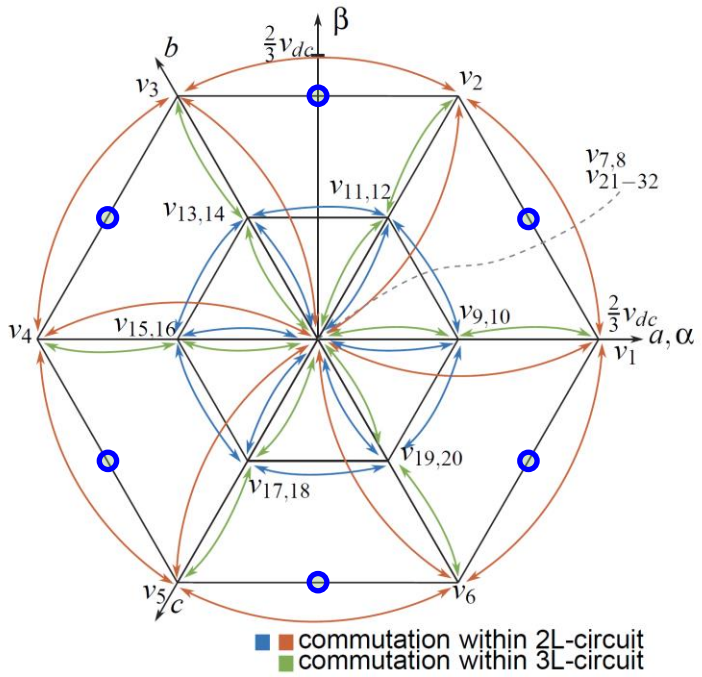
Sparse NPC 3-Level Inverter (3)

FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

- *Application of Low Sw. & Cond. Loss 650V GaN Technology for 800V DC-Link*
- *Redundant Voltage Vectors Allow Control of Neutral Point Voltage*
- *Avg. Sw. Frequency of GaN HEMTs & Si IGBT → Factor 6*

- *Piepenbreier (2018)*





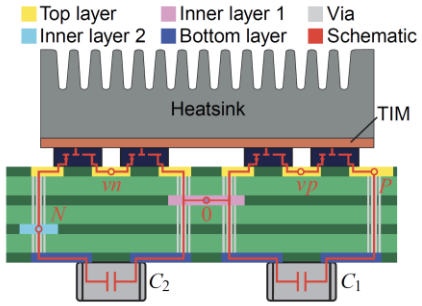
- *Missing Sw. States Compared to Full 3L-NPC → 7 Instead of 9 Phase Voltage Levels*
- *Diff. Sw. Schemes → E.g. Avoiding Commutation of 2L-Stage @ Full DC Voltage*

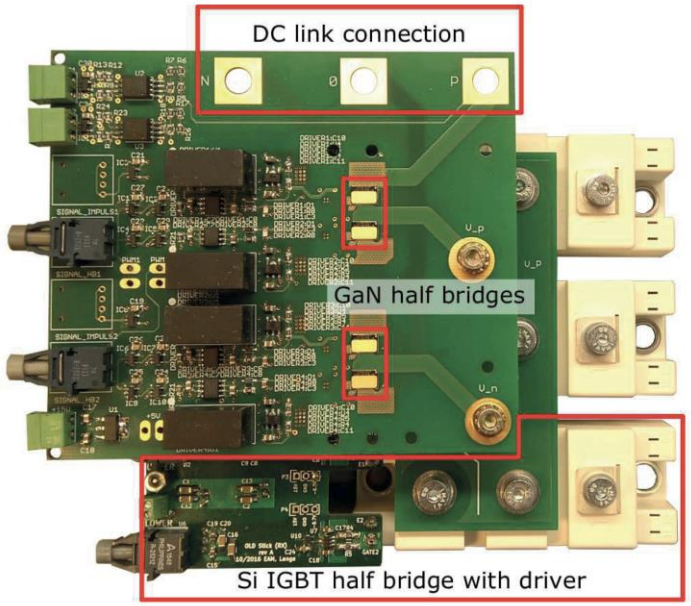
Sparse NPC 3-Level Inverter (4)

FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

- *Demonstrator Using Top-Cooled 650V SMD GaN Half-Bridges & 1200V Si-IGBT Modules*
- *Minimiz. of Commutation Loop by Close Placement of 2L-Inverter Stage & 3L-Source*
- *Vertical Commutation Loop of 3L Input Stage*

– *Piepenbreier (2018)*



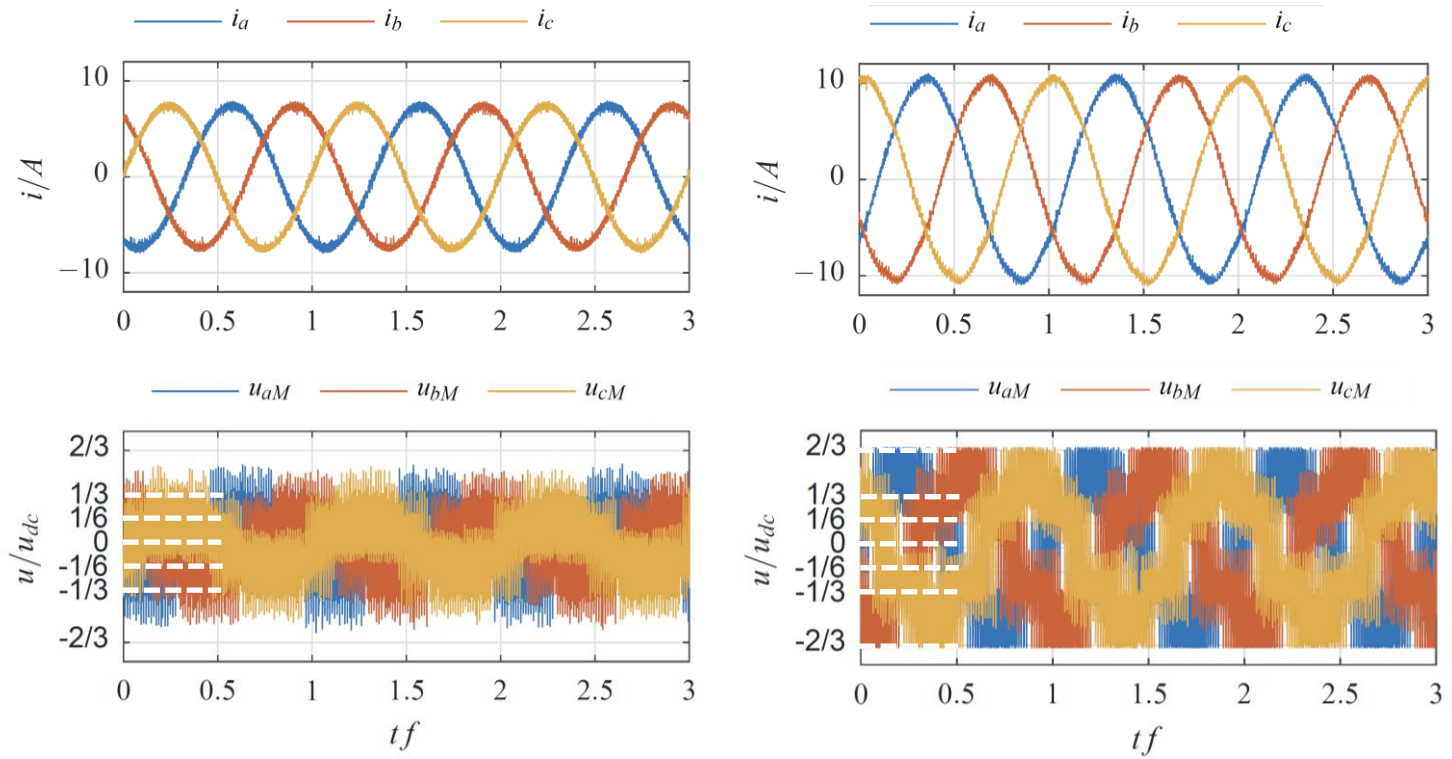


- *10kHz Sampling Frequ.* → *Avg. Sw. Frequencies: 20kHz (GaN) & 3.33kHz (IGBTs)*

Sparse NPC 3-Level Inverter (5)

FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

- ***Experimental Results → Phase Currents & Phase Voltages*** - *Piepenbreier (2018)*



- ***Analysis for Different Modulation Depths — M=0.49 & M=0.92***

Authors

Johann W. Kolar (M'89–F'10) is a Fellow of the IEEE, an International Member of the US NAE and a Full Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel converter concepts incl. the Vienna Rectifier, has spearheaded the development of x-million rpm motors and has pioneered fully automated multi-objective power electronics design procedures. He has graduated 85 Ph.D. students, has published 1000+ research papers, 4 book chapters, and has filed 200+ patents. He has served as IEEE PELS Distinguished Lecturer from 2012 - 2016. He has received 45 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE PEMC Council Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2021 EPE Outstanding Achievement Award and 2 ETH Zurich Golden Owl Awards for excellence in teaching. The focus of his current research is on ultra-compact/efficient WBG PFC rectifier and inverter systems, ultra-high BW switch-mode power amplifiers, multi-port converters, Solid-State Transformers, multi-functional actuators, ultra-high speed / motor-integrated drives, bearingless motors, ANN-based multi-objective design optimization and Life Cycle Assessment of power electronics systems.

Jonas Huber (S'11–M'16–SM'22) received the MSc (with distinction) degree and the PhD degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2012 and 2016, respectively. Since 2012, he has been with the Power Electronic Systems Laboratory, ETH Zurich and became a Post-Doctoral Fellow, focusing his research interests on the field of solid-state transformers, specifically on the analysis, optimization, and design of high-power multi-cell converter systems, reliability considerations, control strategies, and applicability aspects. From 2017, he was with ABB Switzerland Ltd. as an R&D Engineer designing high-power DC-DC converter systems for traction applications, and later with a Swiss utility company as a Business Development Manager. He then returned to the Power Electronic Systems Laboratory as a Senior Researcher in 2020, extending his research scope to all types of WBG-semiconductor-based ultra-compact, ultra-efficient or highly dynamic converter systems.

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